TOSHIBA Insulated Gate Bipolar Transistor Silicon N Channel IGBT

GT45F123

For PDP-TV Applications

• 5th generation (trench gate structure) IGBT

• Enhancement-mode

Low input capacitance: Cies = 2700pF (typ.)

• Peak collector current: ICP = 200 A (max)

• TO-220SIS package

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Collector-emitter voltage		V _{CES}	300	V	
Gate-emitter voltage		V_{GES}	± 30	V	
Collector current	Pulse (Note 1)	I _{CP}	200	Α	
Collector power dissipation	Tc=25°C	P _C	26	W	
	Ta=25°C	L.C.	2		
Junction temperature		Tj	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e.

Unit: mm

43.2±0.2

10±0.3

A

2.7±0.2

1.14±0.15

2.54

2.54

2.54

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2. Collector
3. Emitter

TOSHIBA

2-10U1C

Weight: 2 g (typ.)

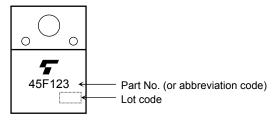
operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Rating	Unit	
Thermal resistance , junction to case $\label{eq:Tc} (\text{Tc} = 25^{\circ}\text{C})$	R _{th (j-c)}	4.8	°C/W	
Thermal resistance , junction to ambient $\label{eq:Ta} (\text{Ta} = 25^{\circ}\text{C})$	R _{th (j-a)}	62.5	°C/W	

Marking



Note 1: I_{CP} maximum rating(200A) is limited by pulse width (3 μs).

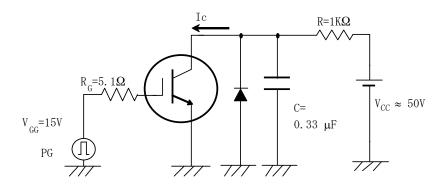
Electrical Characteristics (Ta = 25°C)

Charac	teristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GES}	$V_{GE} = \pm 30 \text{ V}, V_{CE} = 0 \text{V}$	_	_	± 100	nA
Collector cut-off current		I _{CES}	V _{CE} = 300 V, V _{GE} = 0V	_	_	0.5	mA
Emitter-collector voltage		V _{ECS}	I _E = 0.5A, V _{GE} = 0V (Note2)	15	_	_	V
Gate-emitter cut-off voltage		V _{GE} (OFF)	I _C = 10 mA, V _{CE} = 5 V	3.0	4.5	5.5	V
Collector-emitter saturation voltage		V _{CE} (sat) (1)	I _C = 45 A, V _{GE} = 15 V	_	1.35	1.6	V
Collector-emitter saturation voltage		V _{CE} (sat) (2)	I _C = 120 A, V _{GE} = 15 V	_	1.95	2.4	V
Collector-emitter saturation voltage		V _{CE} (sat) (3)	I _C = 200 A, V _{GE} = 15 V	_	2.6	3.3	V
Input capacitance Reverse transfer capacitance		C _{ies}	V _{CE} = 10 V, V _{GE} = 0V, f = 1 MHz	_	2700	_	pF
		C _{res}		_	155	_	
Output capacitance		C _{oes}		_	225	_	
Switching time (Resistance load)	Rise time	t _{r (1)}	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	_	180	_	ns
	Turn-on time	t _{on(1)}		_	230	_	
	Fall time	t _f			200	300	
	Turn-off time	t _{off}		_	290	_	
Switching time (Discharge mode)	Rise time	t _{r (2)}	$V_{CC} \approx 50V$, I_{CP} =100A $V_{GG} = 15V/0V$, R_G =5.1 Ω (Note 3)	_	125	_	ns
	Turn-on time	t _{on(2)}		_	150	_	
Total gate charge (gate-emitter plus gate-drain)		Qg	V _{CE} = 300 V, V _{GE} = 15V, I _C = 120 A	_	110	_	nC

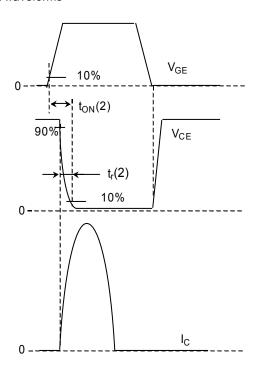
Note 2 : Pulse width $\approx 80~\mu s$ (duty $\approx 0.1\%).$

Note 3: Switching time measurement circuit and input/output waveforms.

< Switching circuit of discharge mode>



< Measurement waveforms >



Caution on handling

This MOS gate device is sensitive to electrostatic discharge (ESD).

When handling the device, be sure that the environment is protected against static electricity.

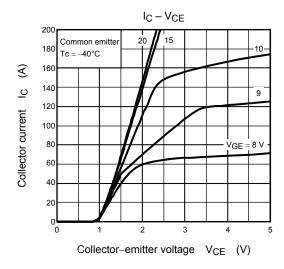
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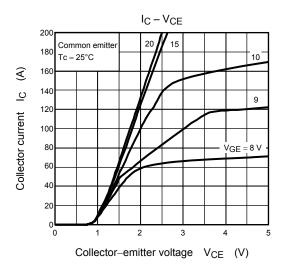
Caution in design

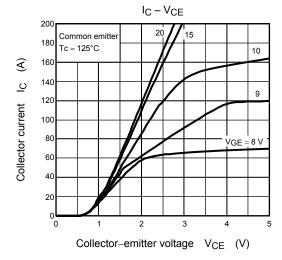
This devise is designed for use in PDP-TVs.

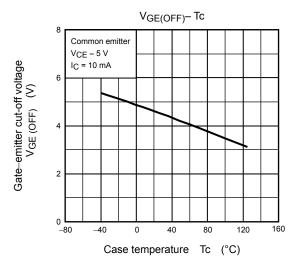
Please contact our sales section if the device is intended for any other use.

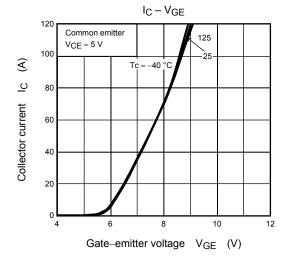
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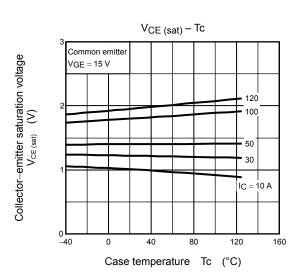


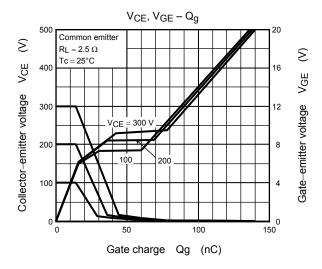


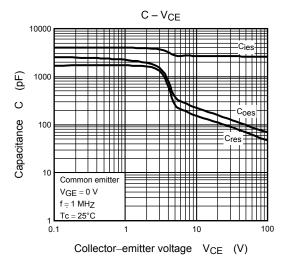


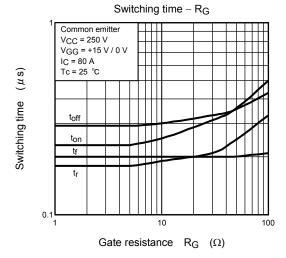


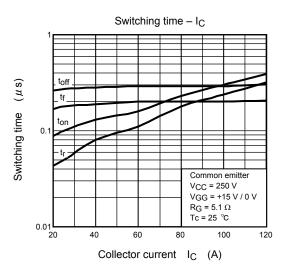


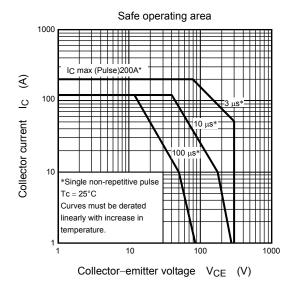


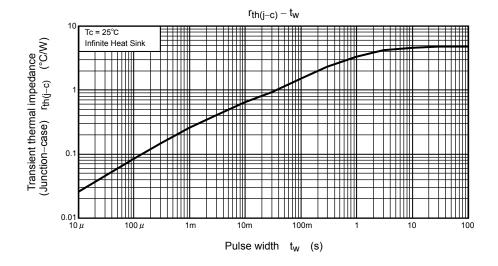












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