Ordering number : EN5835

CMOS IC

LC75374E

Electronic Volume and Tone Control for Car Stereos

Overview

The LC75374E is an electronic volume and tone control circuit that provides volume, balance, fader, bass and treble, super bass, input switching, and input and output level controls and requires a minimal number of external components to implement these functions.

Functions

- Volume: 0dB to –79dB (in 1-dB steps) and –∞dB for a total of 81 positions.
  A balance function can be implemented by controlling the left and right channels independently.
- Fader: Allows either the rear or the front channel outputs to be attenuated over 16 positions.
  (0 to –20dB in 2dB steps, –20 to –25dB in a 5dB step, –25 to –45dB in 10dB steps, –60dB, and –∞dB for a total of 16 positions.)
- Bass and treble: NF-type tone control circuits are formed using external CR circuits. The bass and treble can be controlled from 0dB to +11.9dB (in 1.7dB steps) for a total of 15 positions.
- Input gain: The input signal can be amplified by 0dB to +18.75dB (in 1.25dB steps).
- Output gain: The fader output can be set to one of three settings: 0dB, +6.5dB, or +8.5dB.
- Input switching: Both the left and right channels can be selected from one of four inputs.
- Super bass: This circuit provides peaking characteristics (T type characteristics) and 11 position settings.

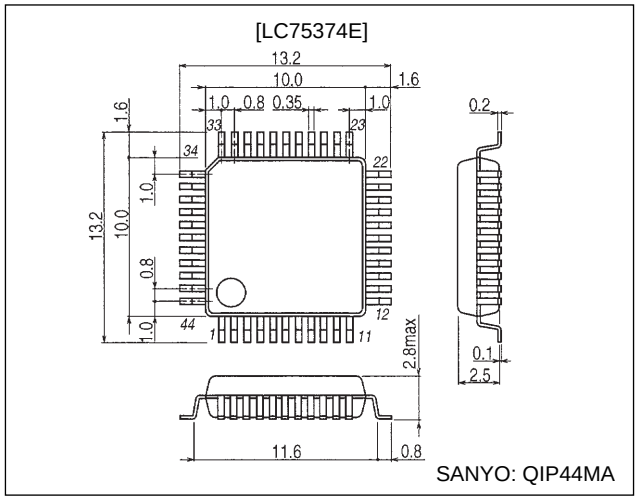
Features

- On-chip buffer amplifiers minimizes the number of external components.
- Built-in reference voltage generator for the analog ground.
- All controls can be set using the serial data input circuit (CCB).

Package Dimensions

unit: mm

3148-QIP44MA



- **CCB is a trademark of SANYO ELECTRIC CO., LTD.**
- **CCB is SANYO's original bus format and all the bus addresses are controlled by SANYO.**

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Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	11	V
Maximum input voltage	V_{IN} max	CL, DI, CE	V_{SS} – 0.3 to V_{DD} + 0.3	V
Allowable power dissipation	Pd max	When Ta ≤ 85°C and mounted on a printed circuit board	720	mW
Operating temperature	Topr		–40 to +85	°C
Storage temperature	Tstg		–50 to +125	°C

Allowable Operating Ranges at Ta = –40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	7.5		9.7	V
High-level input voltage	V_{IH}	CL, DI, CE	4.0		V_{DD}	V
Low-level input voltage	V_{IL}	CL, DI, CE	V_{SS}		1.0	V
Input voltage amplitude	V_{IN}	CL, DI, CE, LVRIN, RVRIN, L1 to L4, R1 to R4, LFIN, RFIN, LSIN, RSIN	V_{SS}		V_{DD}	Vp-p
Input pulse width	tϕW	CL	1			µs
Setup time	t_{setup}	CL, DI, CE	1			µs
Hold time	t_{hold}	CL, DI, CE	1			µs
Operating frequency	fopg	CL			500	kHz

Electrical Characteristics at Ta = 25°C, V_{DD} = 8 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Input Block]						
Maximum input gain	Gin max			+18.75		dB
Step resolution	Gstep			+1.25		dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LSEL0, RSEL0 : R_L = 10 kΩ, f = 1 kHz, V_{IN} = 1 Vrms		46		Ω
[Output Block]						
Maximum output gain	Gout max			+8.5		dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LFOUT, LROUT, RFOUT, RROUT : R_L = 10 kΩ, f = 1 kHz, V_{IN} = 1 Vrms		35		Ω
[Volume Control Block]						
Step resolution	ATstep			1		dB
Step error	ATerr	STEP = 0 dB to –20 dB	–1	0	+1	dB
		STEP = –20 dB to –50 dB	–3	0	+3	dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LTOUT, RTOUT : R_L = 10 kΩ, f = 1 kHz, V_{IN} = 1 Vrms		46		Ω
[Fader Volume Control Block]						
Step resolution	ATstep	STEP = 0 dB to –20 dB		2		dB
		STEP = –20 dB to –25 dB		5		dB
		STEP = –25 dB to –45 dB		10		dB
Step error	ATerr	STEP = 0 dB to –45 dB	–2	0	+2	dB
		STEP = –45 dB to –60 dB	–3	0	+3	dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LFOUT, LROUT, RFOUT, RROUT : R_L = 10 kΩ, f = 1 kHz, V_{IN} = 1 Vrms		46		Ω
[Bass and Treble Control Block]						
Bass control range	Gbass	Max. Boost/Cut	±8	±11.9	±13	dB
Treble control range	Gtre	Max. Boost/Cut	±8	±11.9	±13	dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LTOUT, RTOUT : R_L = 10 kΩ, f =1 kΩ, V_{IN} = 1 Vrms		46		Ω

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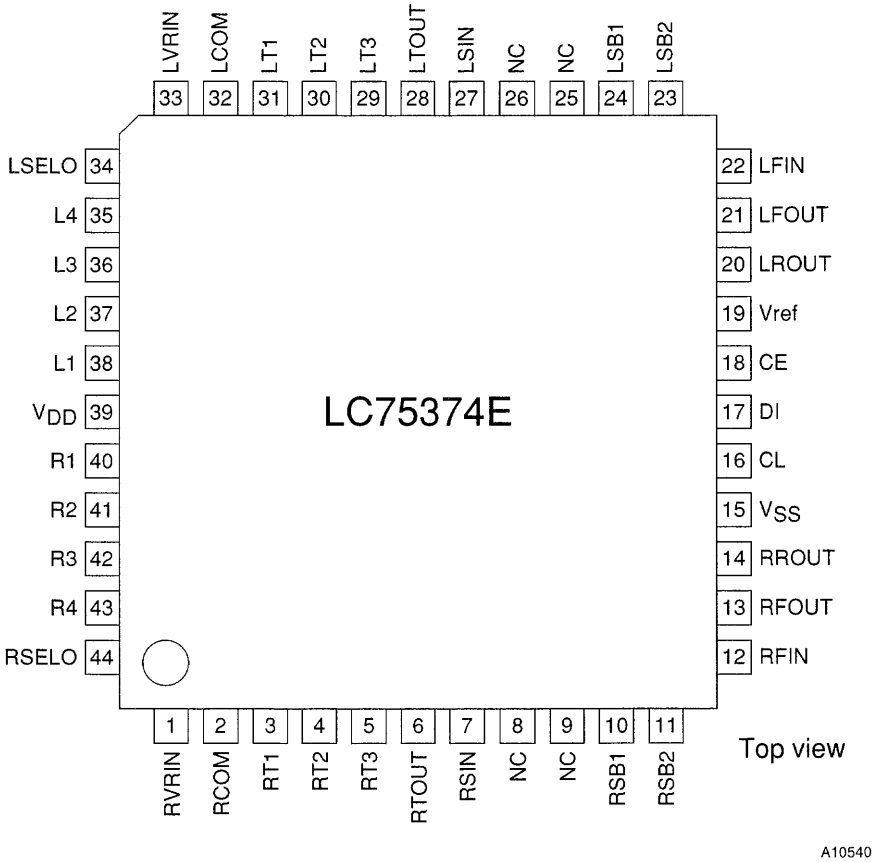
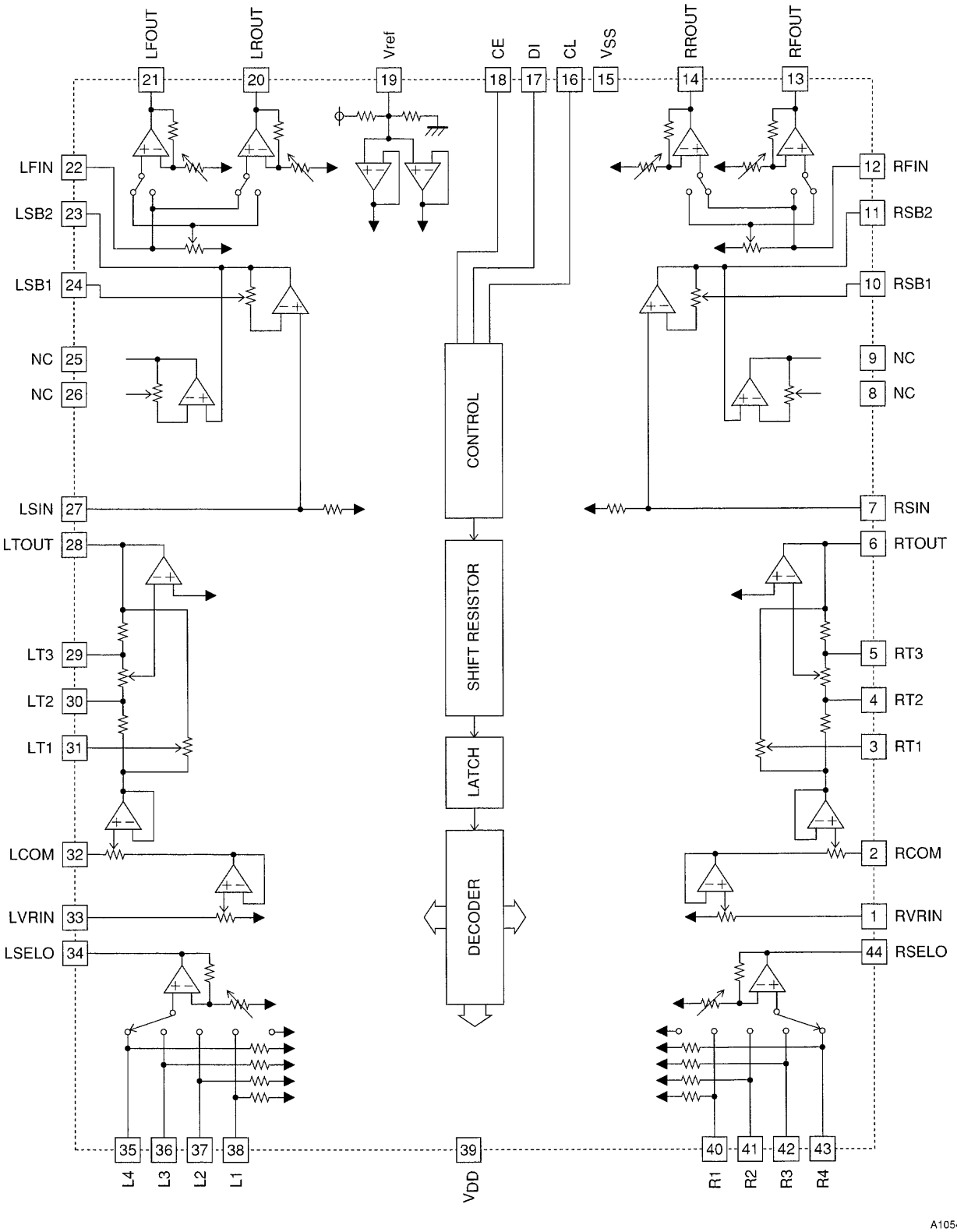
Electrical Characteristics at Ta = 25°C, V_{DD} = 8 V, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Super-Bass Block] (T type)						
Control range	Crange	Max. Boost		+20		dB
Step resolution	ATstep			+2.0		dB
Output load resistance	R_L		10			kΩ
Output impedance	R_O	LSB2, RSB2 : R_L = 10 kΩ, f = 1 kHz, V_{IN} = 1 Vrms		70		Ω
[Overall]						
Total harmonic distortion	THD	V_{IN} = 1 Vrms, f = 1 kHz, All controls flat overall		0.003	0.01	%
Crosstalk	CT	V_{IN} = 1 Vrms, f = 1 kHz, All controls flat overall, Rg = 1 kΩ		80.5		dB
Output at maximum attenuation	Vo min	V_{IN} = 1 Vrms, f = 1 kHz, Main volume setting: –∞		–80		dB
Output noise voltage	V_N1	All controls flat overall, (IHF-A), Rg = 1 kΩ		8		μV
	V_N2	All controls flat overall, (DIN-AUDIO), Rg = 1 kΩ		10		μV
High-level input voltage	I_{IH}	CL, DI, CE, V_{IN} = 8 V			10	μA
Low-level input voltage	I_{IL}	CL, DI, CE, V_{IN} = 0 V	–10			μA

Pin Assignment

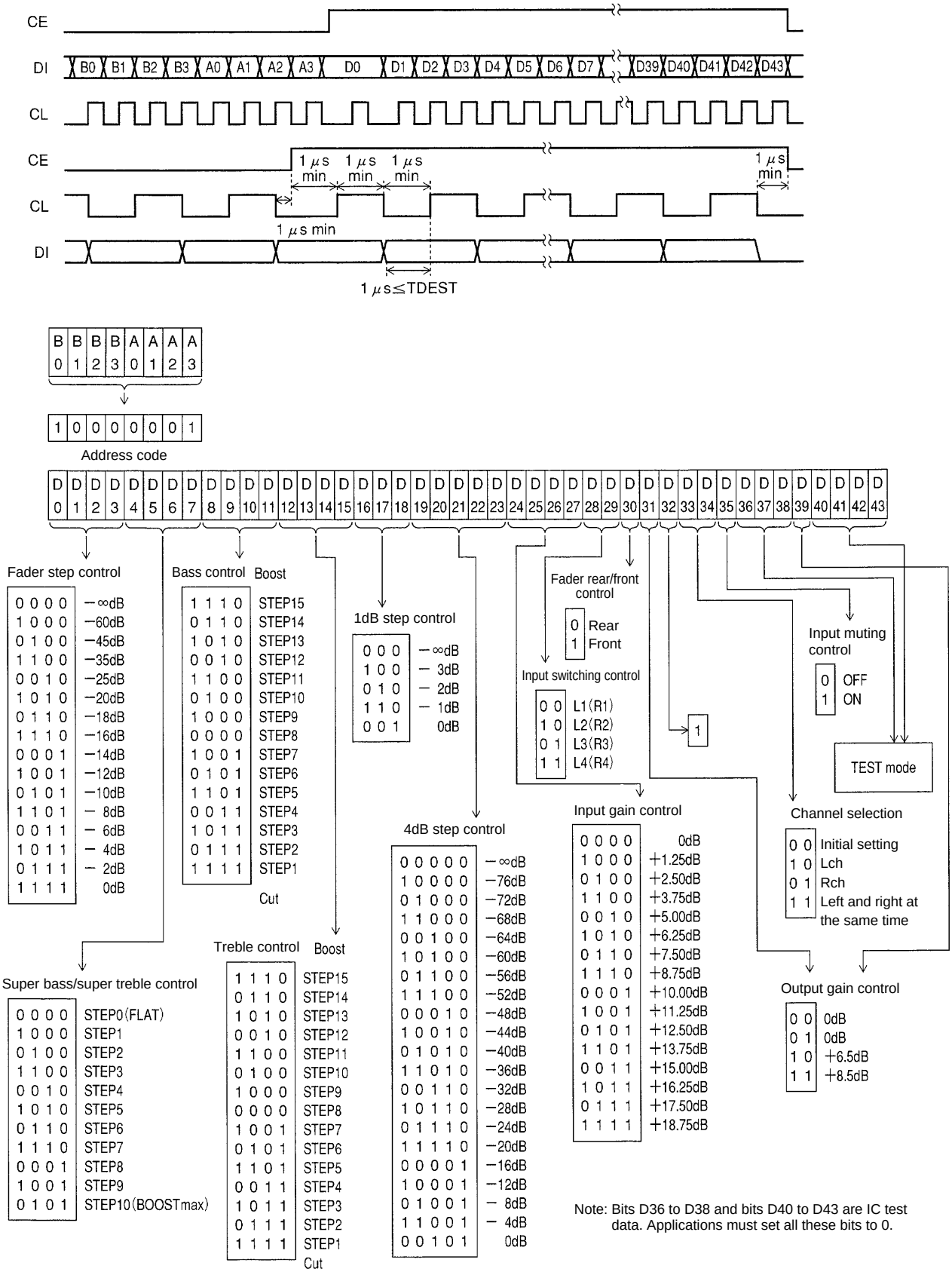


Equivalent Circuit



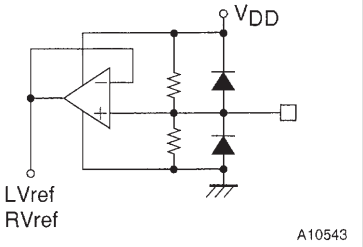
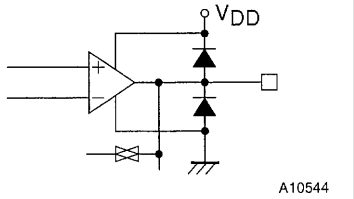
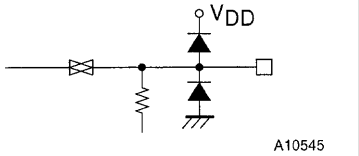
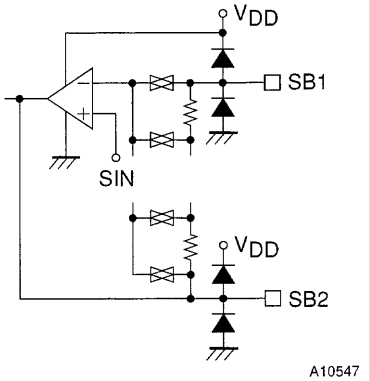
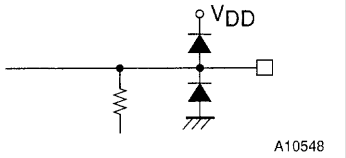
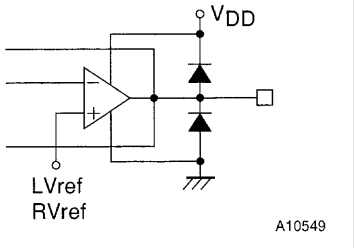
Control System Timing and Data Format

Applications must input the stipulated serial data to the CE, CL, and DI pins to control the LC75374E. The data consists of a total of 52 bits, of which 8 bits are address and 44 bits are data.



Note: Bits D36 to D38 and bits D40 to D43 are IC test data. Applications must set all these bits to 0.

Pin Functions

Pin No.	Pin	Description	Notes
19	Vref	• Supply voltage generator (0.525 × V_{DD}) used for the analog ground. A capacitor must be connected between Vref and V_{SS} to remove power supply ripple.	
20 21 14 13	LROUT LFOUT RROUT RFOUT	• Fader outputs. The front and rear outputs can be attenuated independently.	
22 12	LFIN RFIN	• Fader inputs • These inputs must be driven by low-impedance circuits.	
24 23 10 11	LSB1 LSB2 RSB1 RSB2	• Left channel super bass compensation capacitor connection • Left channel super bass output and compensation capacitor connection • Right channel super bass compensation capacitor connection • Right channel super bass output and compensation capacitor connection	
22 7	LSIN RSIN	• Super bass input • These inputs must be driven by low-impedance circuits.	
28 6	LTOUT RTOUT	• Tone control outputs	

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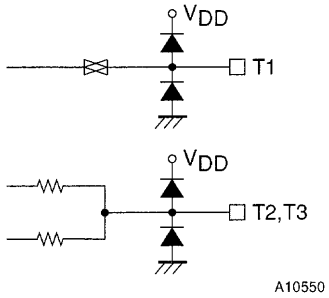
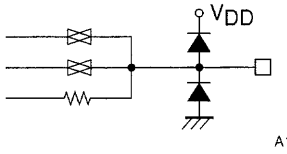
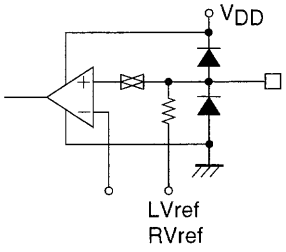
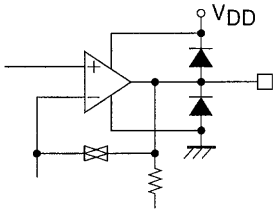
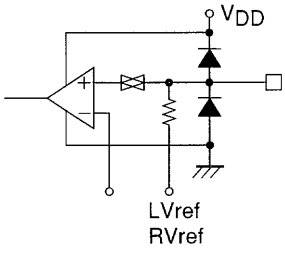
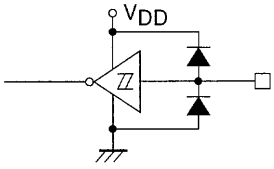
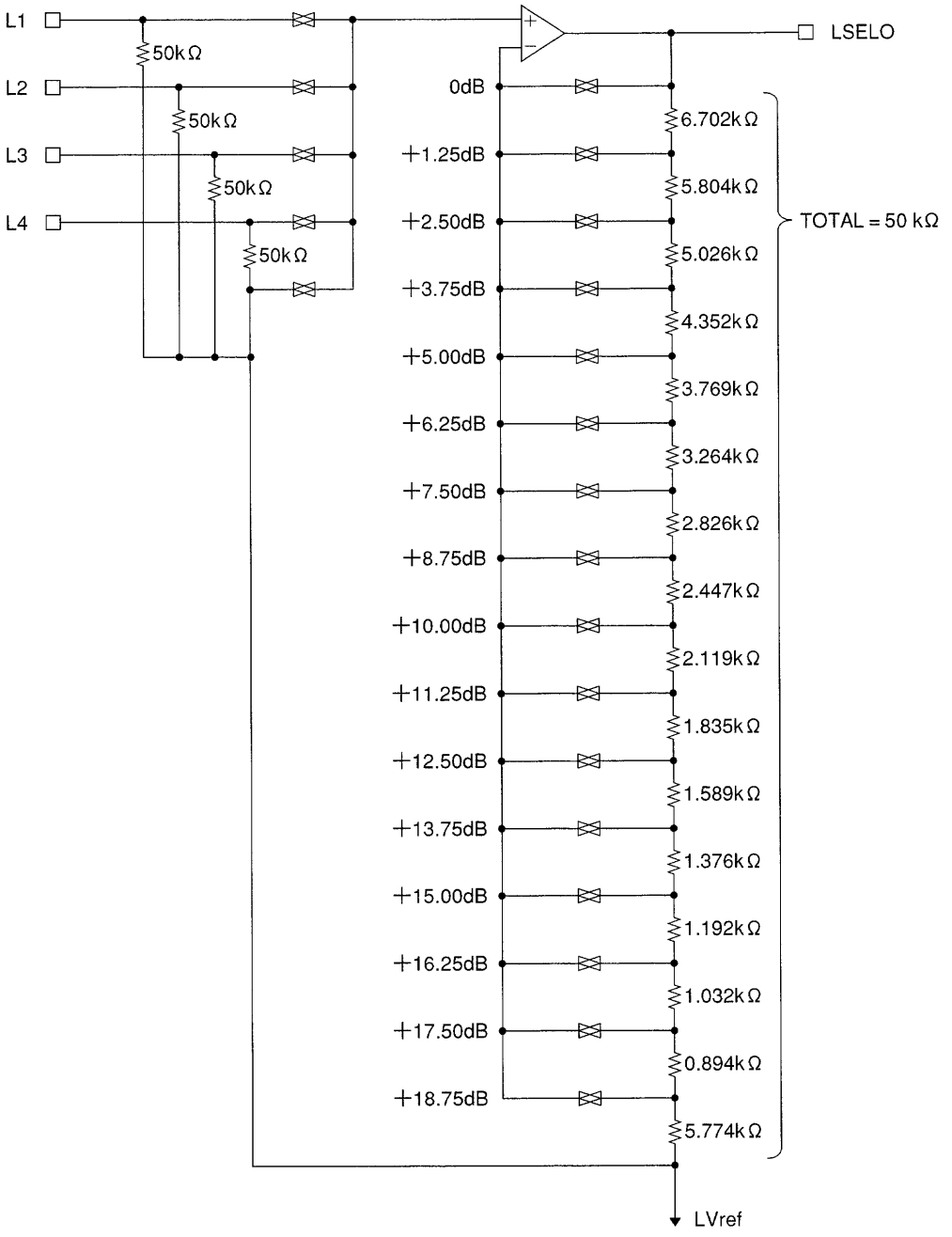
Pin No.	Pin	Description	Notes
31 30 29 3 4 5	LT1 LT2 LT3 RT1 RT2 RT3	• Tone control circuit bass and treble compensation capacitor connections. Connect the high band compensation capacitors between the pins T1 and T2. Connect the low band compensation capacitors between the pins T2 and T3.	
32 2	LCOM RCOM	• 1dB volume control common connections	
33 1	LVRIN RVRIN	• 4dB volume control inputs • These inputs must be driven by low-impedance circuits.	
34 44	LSEL0 RSEL0	• Input selector outputs	
38 37 36 35 40 41 42 43	L1 L2 L3 L4 R1 R2 R3 R4	• Signal inputs	
39	V_{DD}	• Power supply	
15	V_{SS}	• Ground	
16 17	CL DI	• Serial data and clock inputs used for transferring control data	
18	CE	• Chip enable input. Data is written into the internal latches and the analog switches operate when this pin goes from high to low. Data transfers are enabled when this pin is high.	
8, 26 9, 25	NC	• Unused pins. These pins must be connected to V_{SS}. • Unused pins. These pins must be left open.	

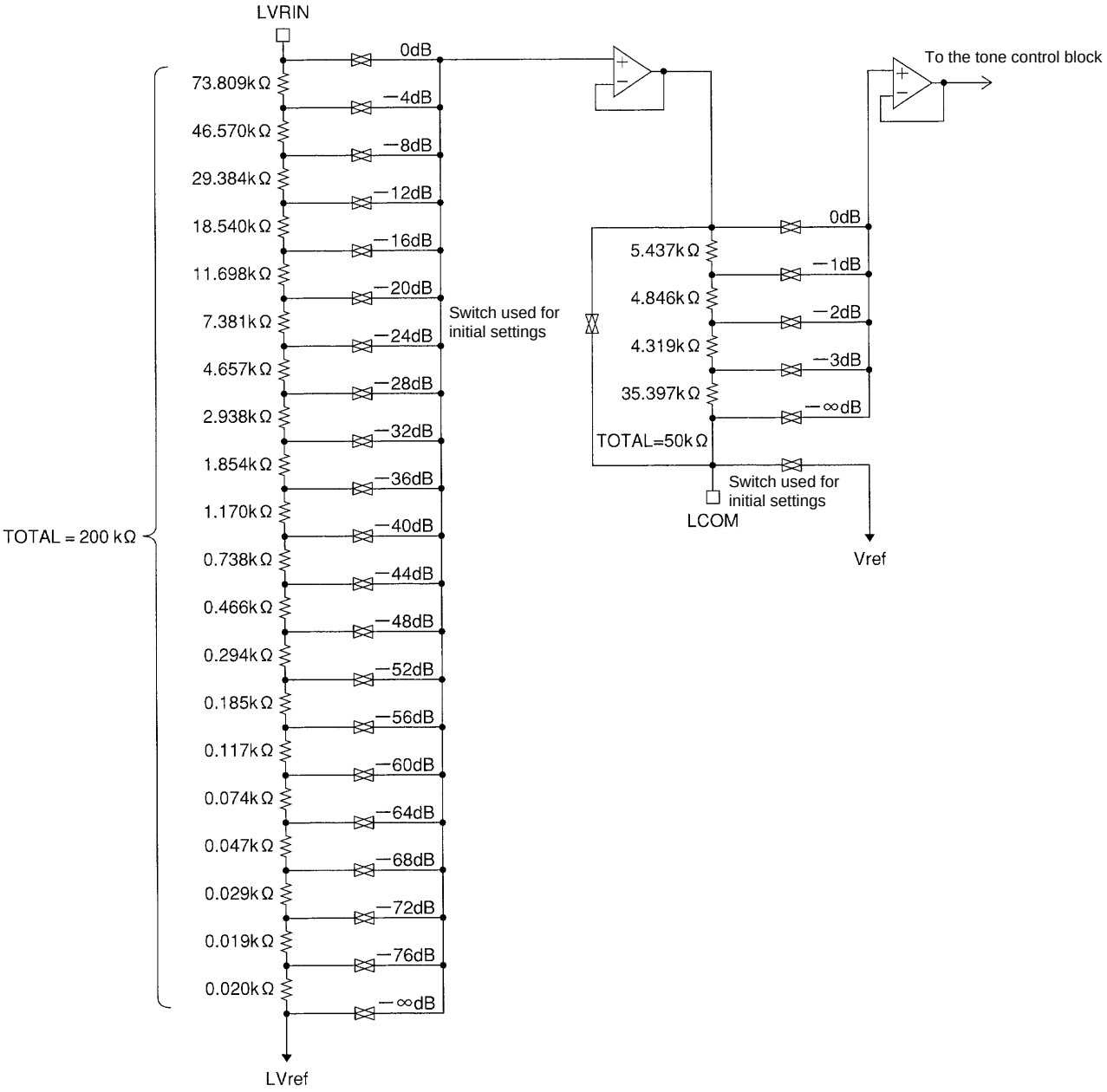
Input Block Equivalent Circuit



A10556

The right channel is identical.

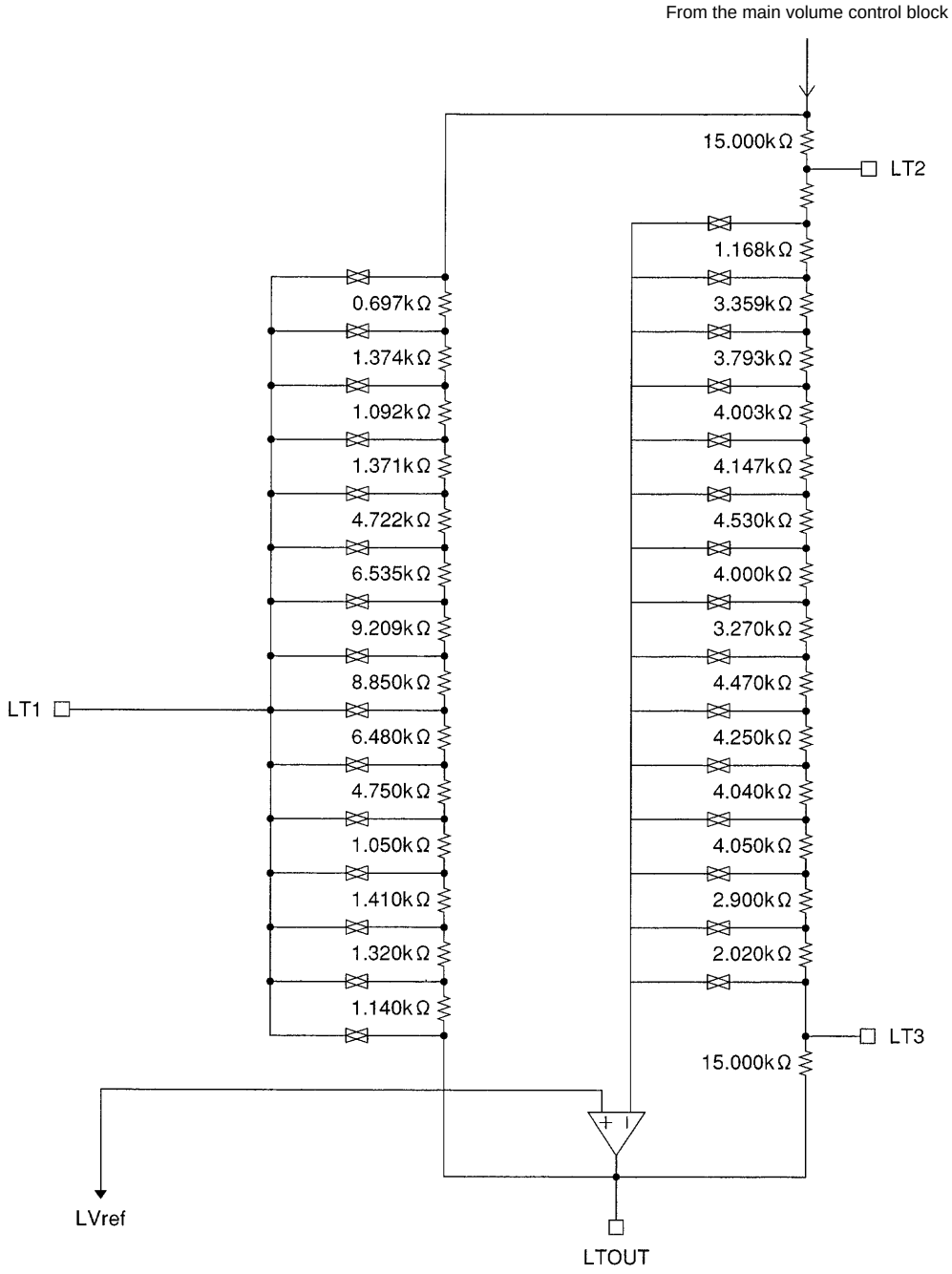
Main Volume Control Block Equivalent Circuit



A10557

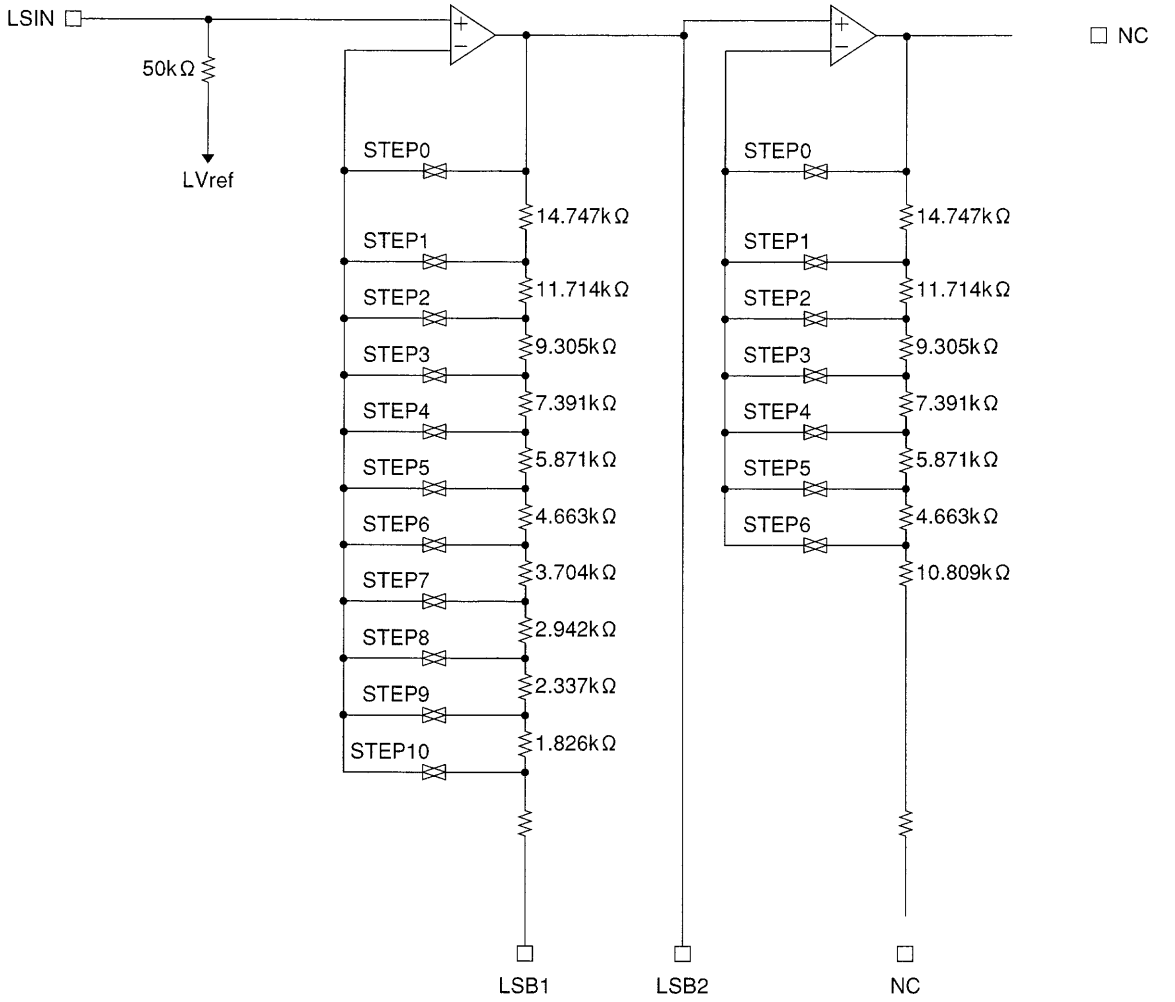
The right channel is identical.

Tone Block Equivalent Circuit



The right channel is identical.

Super Bass Block Equivalent Circuit

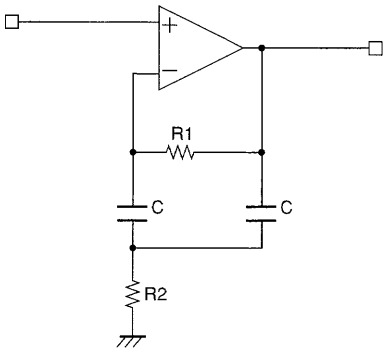


The right channel is identical.

Sample external constant calculations for the super bass (T type) circuit when full boost is used

The external constants required when full boost is used with the super bass block (T type) are calculated as follows.

• Super bass (T type) equivalent circuit



• Calculation

(1) Center frequency

$$f0 = \frac{1}{2\times\pi\times\sqrt{R1\times R2\times C\times C}}$$

(2) Gain

$$G = 20\log\left(1+\frac{R1}{2\times R2}\right)$$

(3) Q

$$Q = \frac{C\times C\times R1}{2\times C}\times\frac{1}{\sqrt{R1\times R2\times C\times C}}$$

Sample calculation
Assume:
R1 = 64.5 kΩ, and
G = 20.65 dB, and
f0 = 72.7 Hz.

• Determine R2
Determine R2 from formula (2).

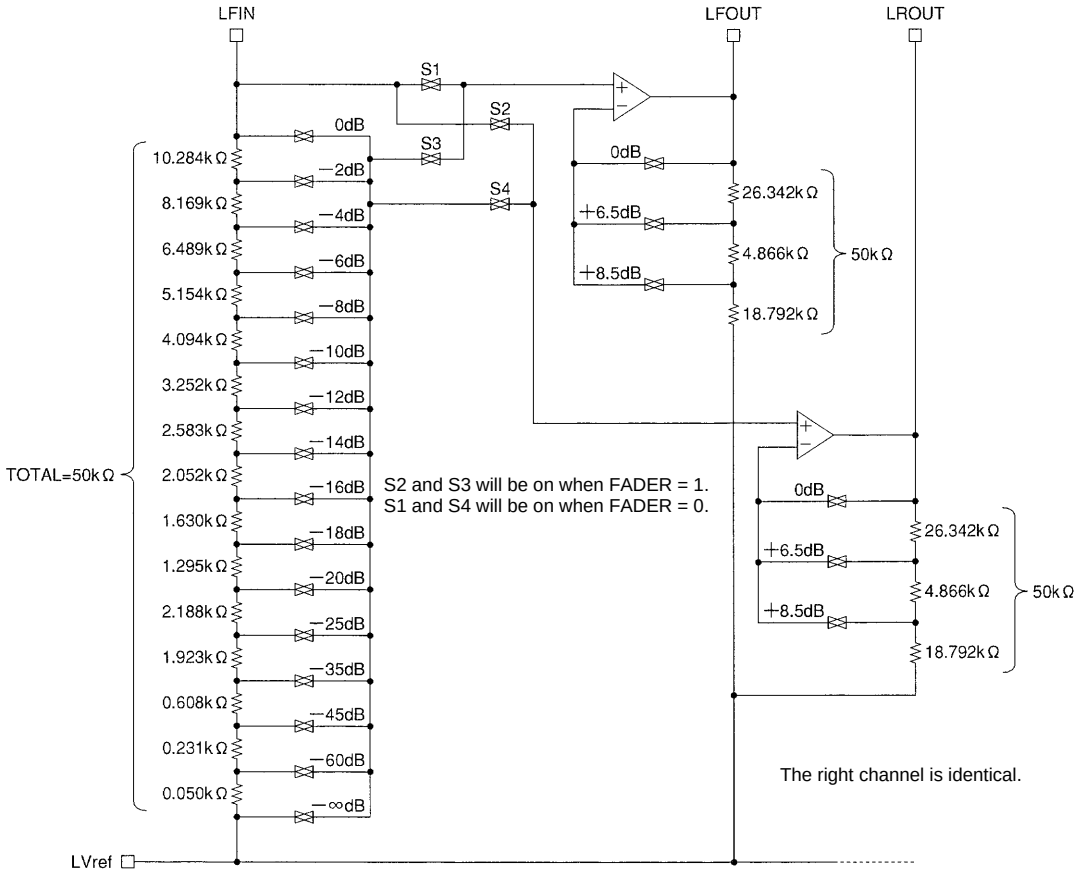
$$R2 = \frac{64.5}{2\times(10.78-1)} \approx 3.3\ (k\Omega)$$

• Determine C
Determine C from formula (1).

$$C = \frac{1}{\sqrt{R1\times R2\times(2\times\pi\times f0)\times(2\times\pi\times f0)}} \approx 0.15\ (\mu F)$$

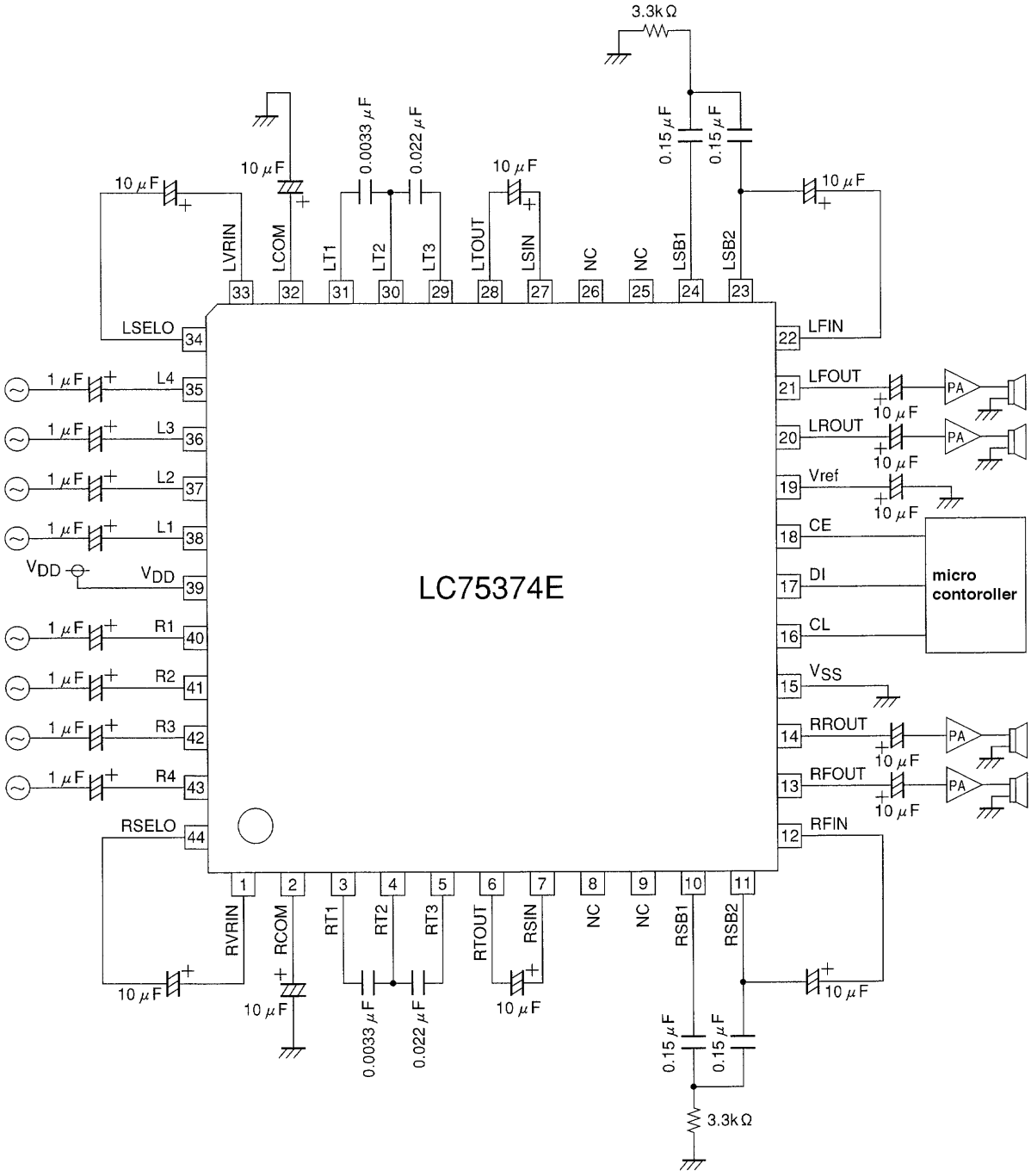
• Determine Q
Determine Q from formula (3).
Here, Q will be 2.21.

Fader Volume Control Block Equivalent Circuit



At the point that data corresponding to –∞ is transferred to the 1dB –step main volume control block, S1 and S2 will go to the open state. S3 and S4 will go to the on state at the same time.

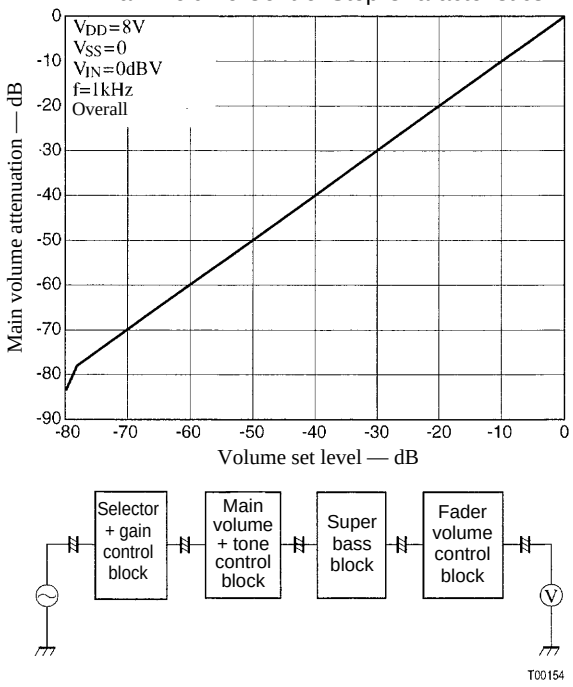
Sample Application Circuit



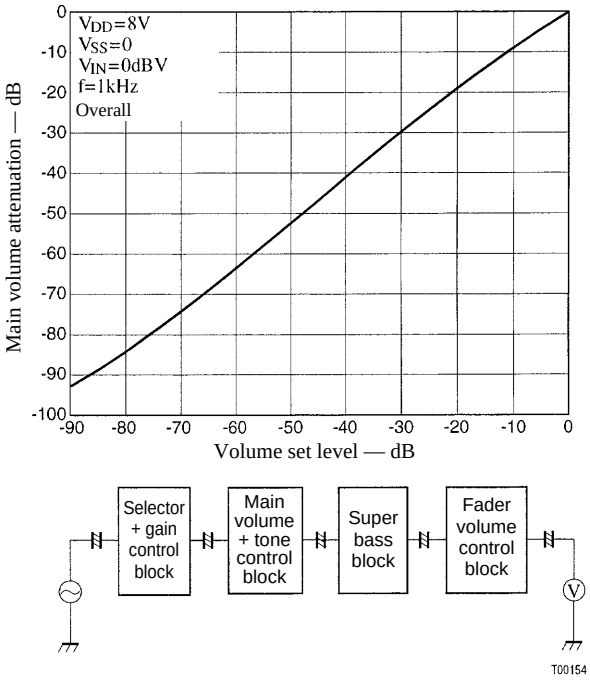
Usage Notes

- The internal analog switches are in undefined states when power is first applied. Applications must therefore use external circuits to mute the output until control data has been transferred.
- When setting up the initial data after power is first applied, applications must first transfer a set of IC initialization data. This initialization data consists of an address field of (10000001) and a data field of all zeros (D0 to D43 = 0). Applications must only send the actual initial data after this initialization data has been sent.
- Applications must either cover the CL, DI, and CE lines with the ground pattern or use shielded cables for these lines to prevent the high-frequency digital signals that are transmitted over these lines from entering the analog signal system.

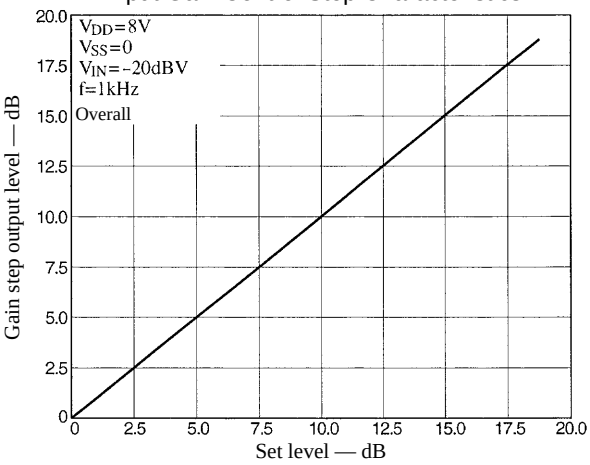
Main Volume Control Step Characteristics

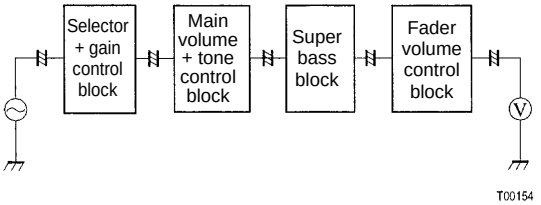


Fader Volume Control Step Characteristics

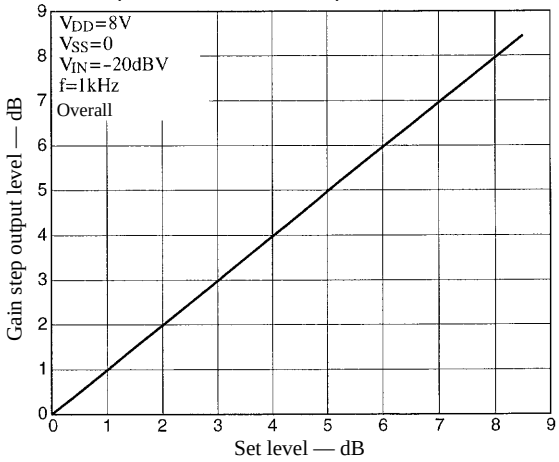


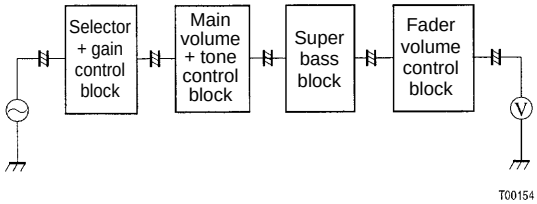
Input Gain Control Step Characteristics



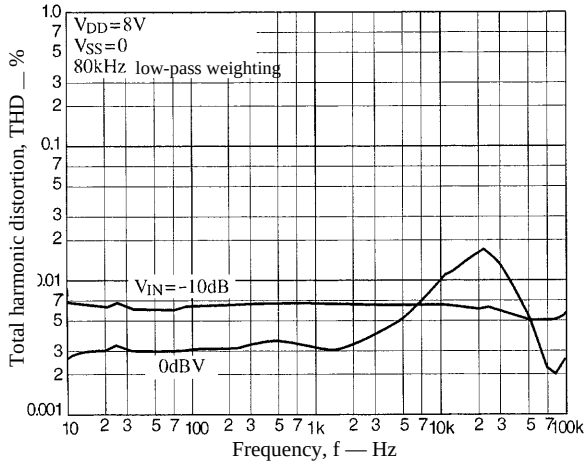


Output Gain Control Step Characteristics

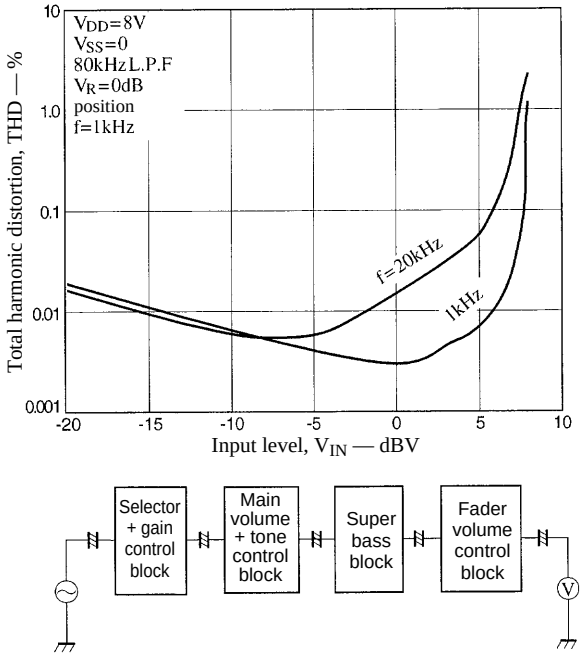




Total Harmonic Distortion - Frequency Characteristics



Total Harmonic Distortion - Input Level Characteristics



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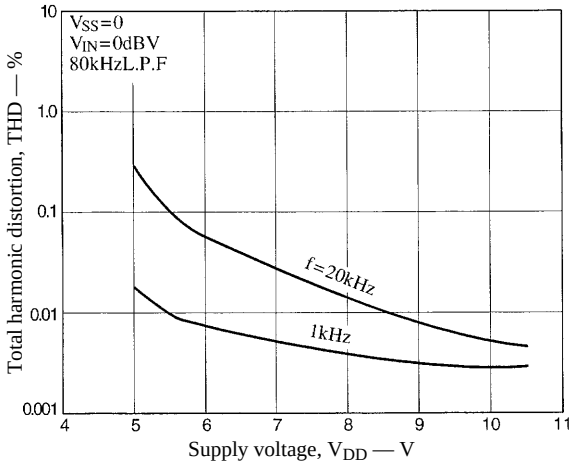
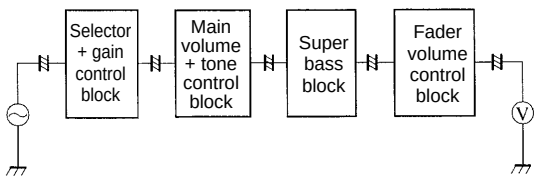
Total Harmonic Distortion - Supply Voltage Characteristics (1)





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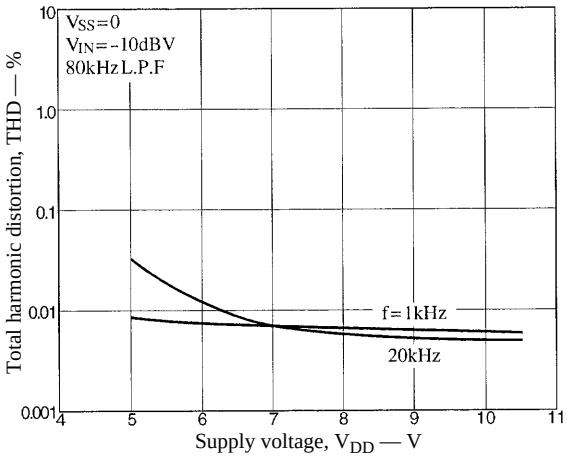
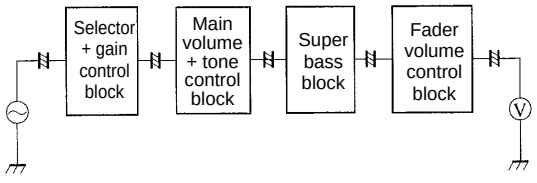
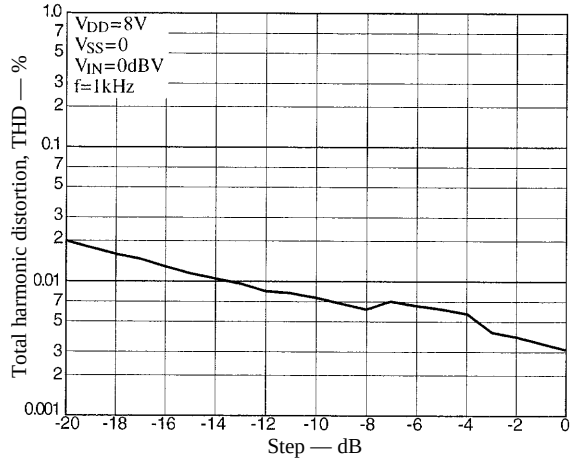
Total Harmonic Distortion - Supply Voltage Characteristics (2)

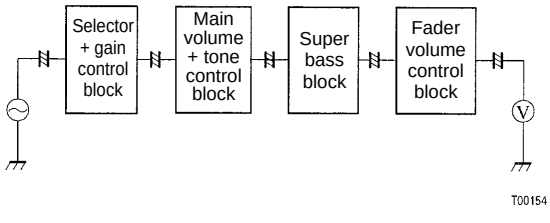




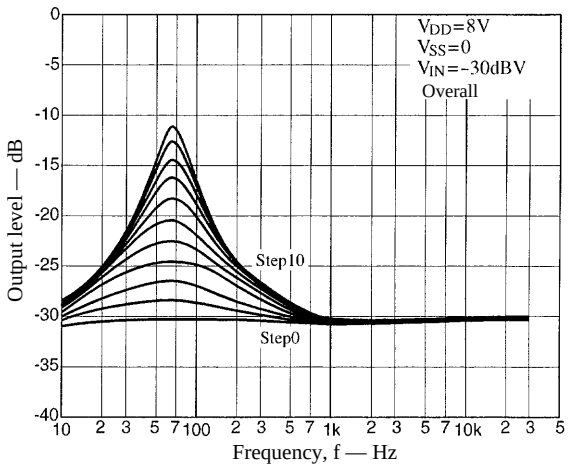
T00154

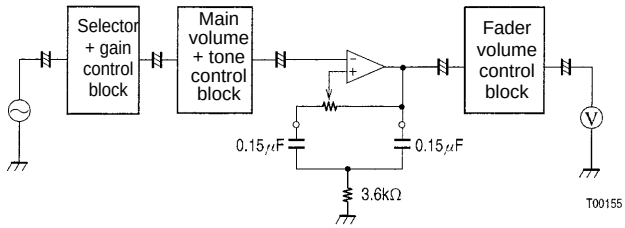
Total Harmonic Distortion – Main Volume Control Step Characteristics



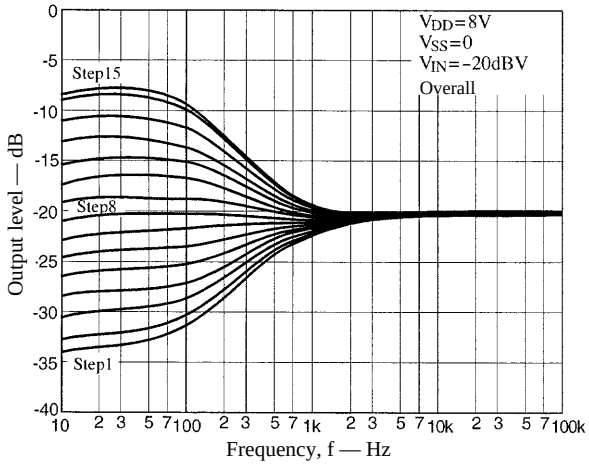


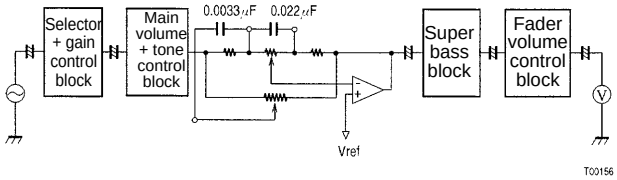
Super Bass Characteristics





Bass Characteristics





Treble Characteristics