International
IOR Rectifier

PD - 94245

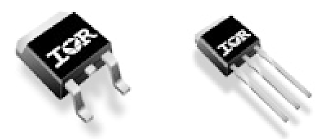
SMPS MOSFET

IRFR15N20D
IRFU15N20D
HEXFET® Power MOSFET

Applications
- High frequency DC-DC converters

V_{DSS}	$R_{DS(on)}$ max	I_D
200V	**0.165Ω**	**17A**

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



D-Pak IRFR15N20D   I-Pak IRFU15N20D

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	17	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	12	
I_{DM}	Pulsed Drain Current ①	68	
P_D @T_C = 25°C	Power Dissipation	140	
P_D @T_A = 25°C	Power Dissipation*	3.0	W
	Linear Derating Factor	0.96	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	8.3	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case	–––	1.04	°C/W
$R_{θJA}$	Junction-to-Ambient (PCB mount)*	–––	50	
$R_{θJA}$	Junction-to-Ambient	–––	110	

Notes ① through ⑤ are on page 10

7/25/01

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	200	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.26	——	V/°C	Reference to 25°C, I_D = 1mA ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.165	Ω	V_{GS} = 10V, I_D = 10A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 200V, V_{GS} = 0V
		——	——	250		V_{DS} = 160V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -30V

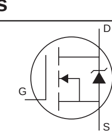
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	4.0	——	——	S	V_{DS} = 50V, I_D = 10A
Q_g	Total Gate Charge	——	27	41	nC	I_D = 10A
Q_{gs}	Gate-to-Source Charge	——	6.9	10		V_{DS} = 160V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	14	21		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	——	9.7	——	ns	V_{DD} = 100V
t_r	Rise Time	——	32	——		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	——	17	——		R_G = 6.8Ω
t_f	Fall Time	——	8.9	——		V_{GS} = 10V ④
C_{iss}	Input Capacitance	——	910	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	170	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	31	——		ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	1380	——		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	——	67	——		V_{GS} = 0V, V_{DS} = 160V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	150	——		V_{GS} = 0V, V_{DS} = 0V to 160V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	260	mJ
I_{AR}	Avalanche Current①	——	10	A
E_{AR}	Repetitive Avalanche Energy①	——	14	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	17	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	68		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 10A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	130	200	ns	T_J = 25°C, I_F = 10A
Q_{rr}	Reverse RecoveryCharge	——	610	920	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

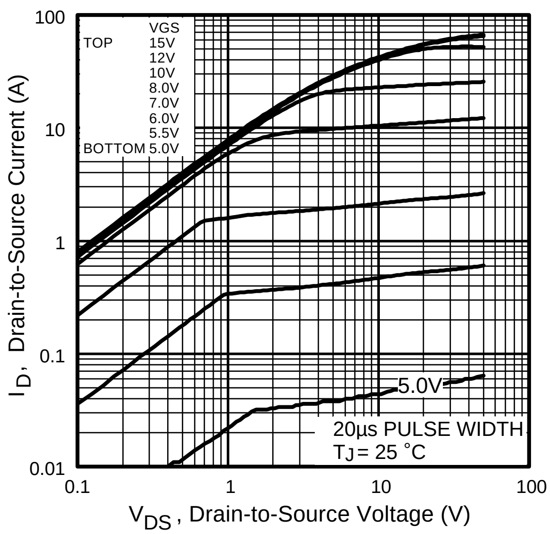


Fig 1. Typical Output Characteristics

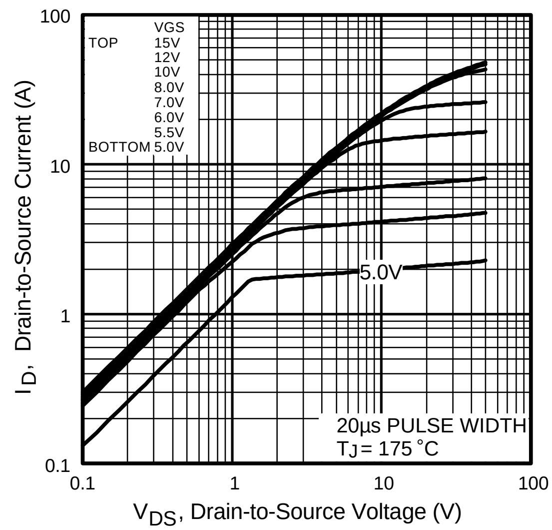


Fig 2. Typical Output Characteristics

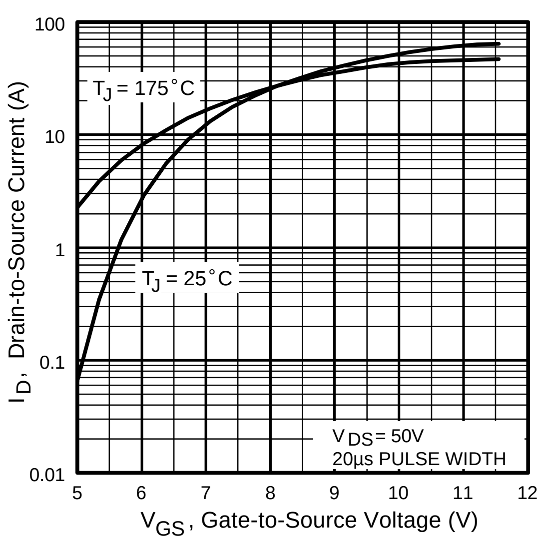


Fig 3. Typical Transfer Characteristics

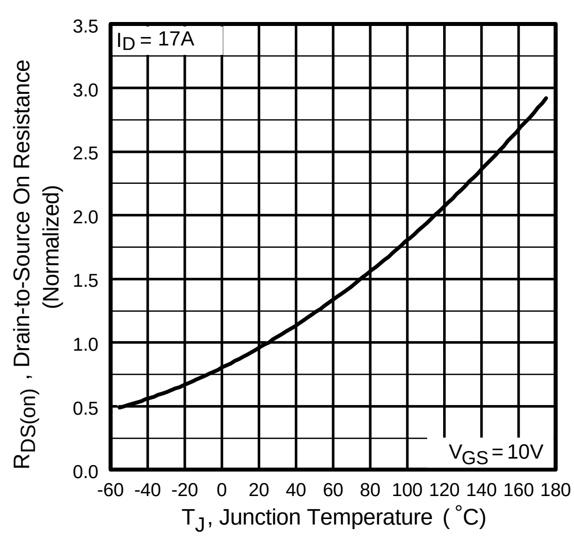


Fig 4. Normalized On-Resistance Vs. Temperature

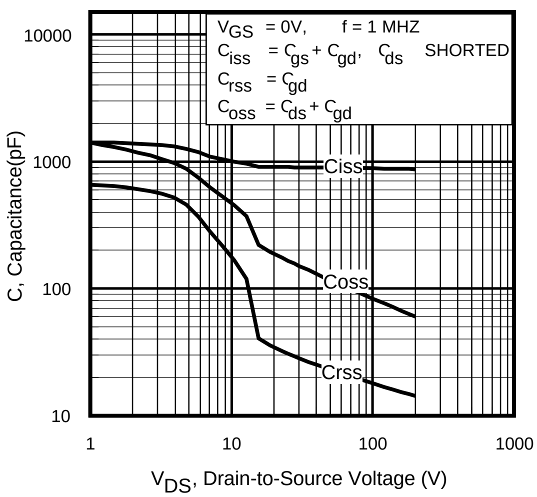


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

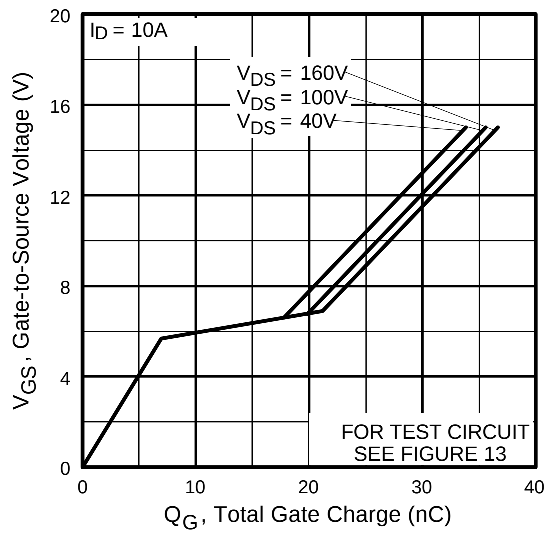


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

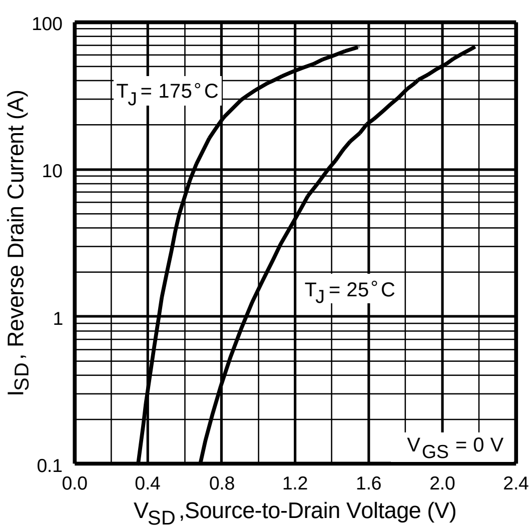


Fig 7. Typical Source-Drain Diode Forward Voltage

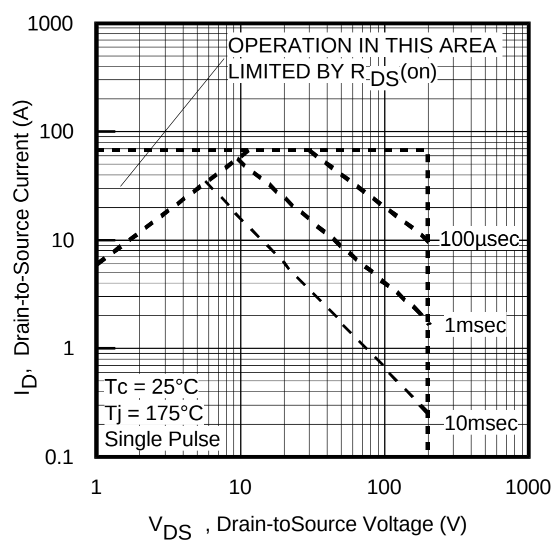


Fig 8. Maximum Safe Operating Area

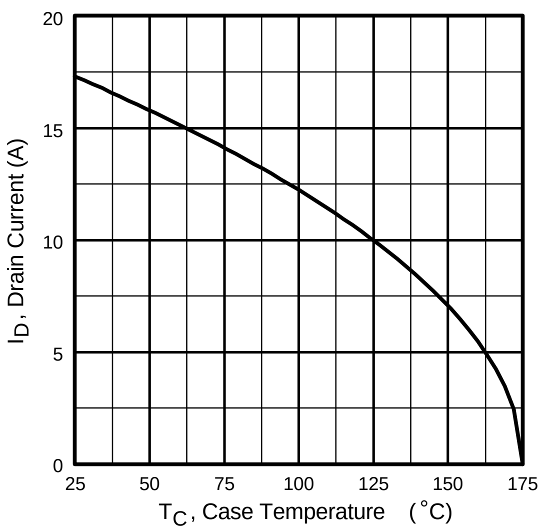


Fig 9. Maximum Drain Current Vs. Case Temperature

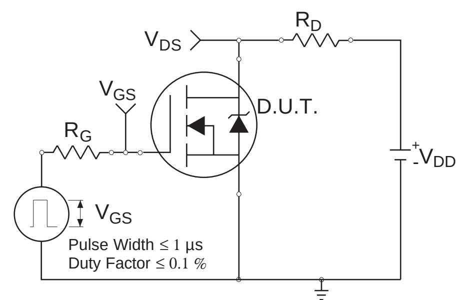


Fig 10a. Switching Time Test Circuit

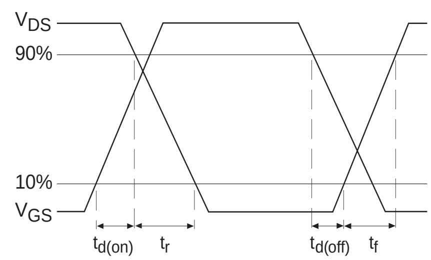


Fig 10b. Switching Time Waveforms

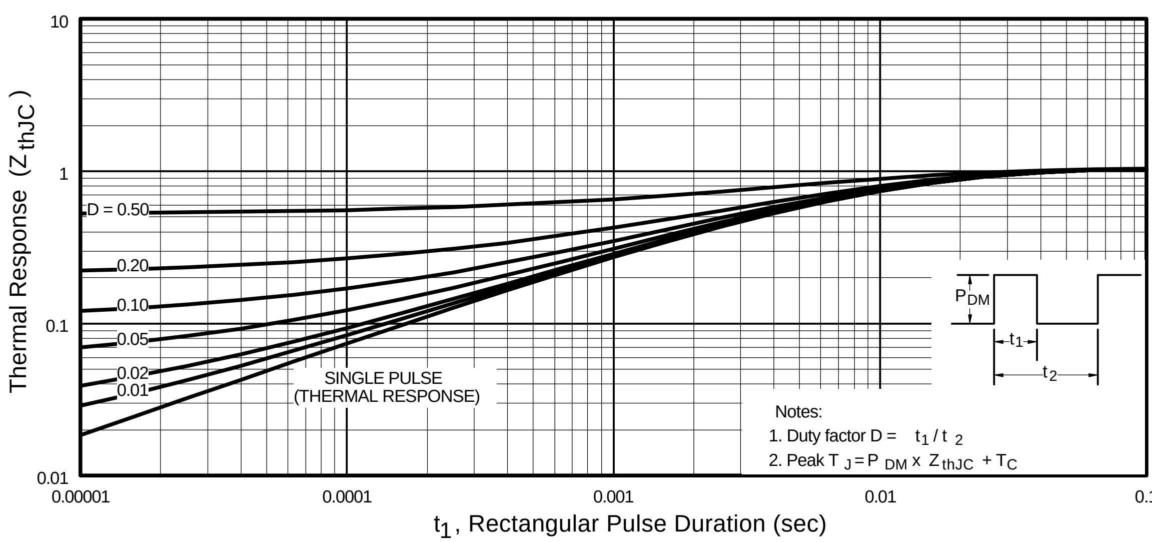


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

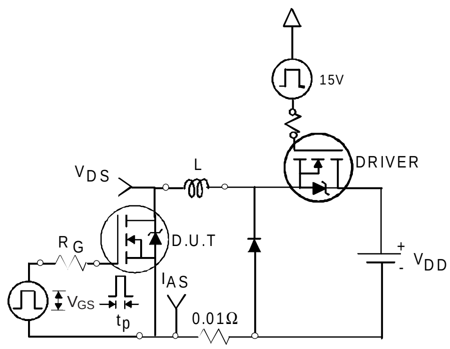


Fig 12a. Unclamped Inductive Test Circuit

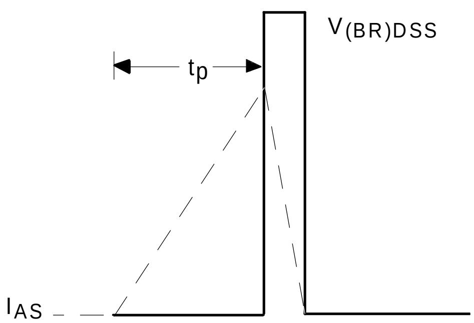


Fig 12b. Unclamped Inductive Waveforms

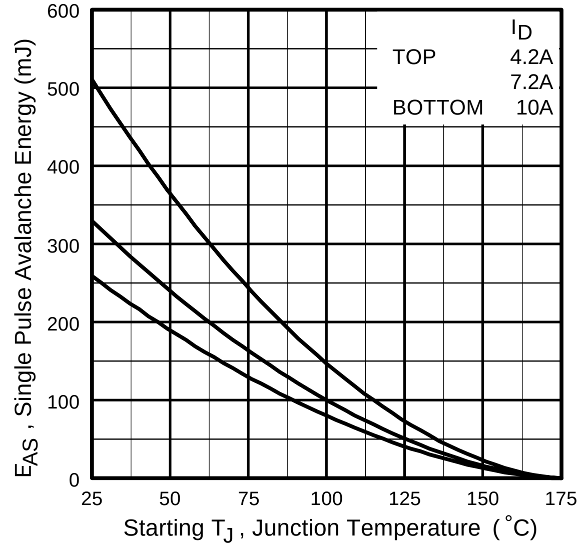


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

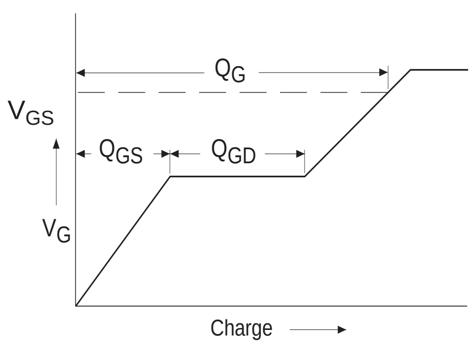


Fig 13a. Basic Gate Charge Waveform

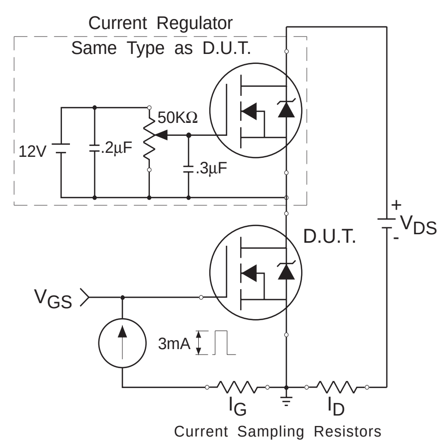
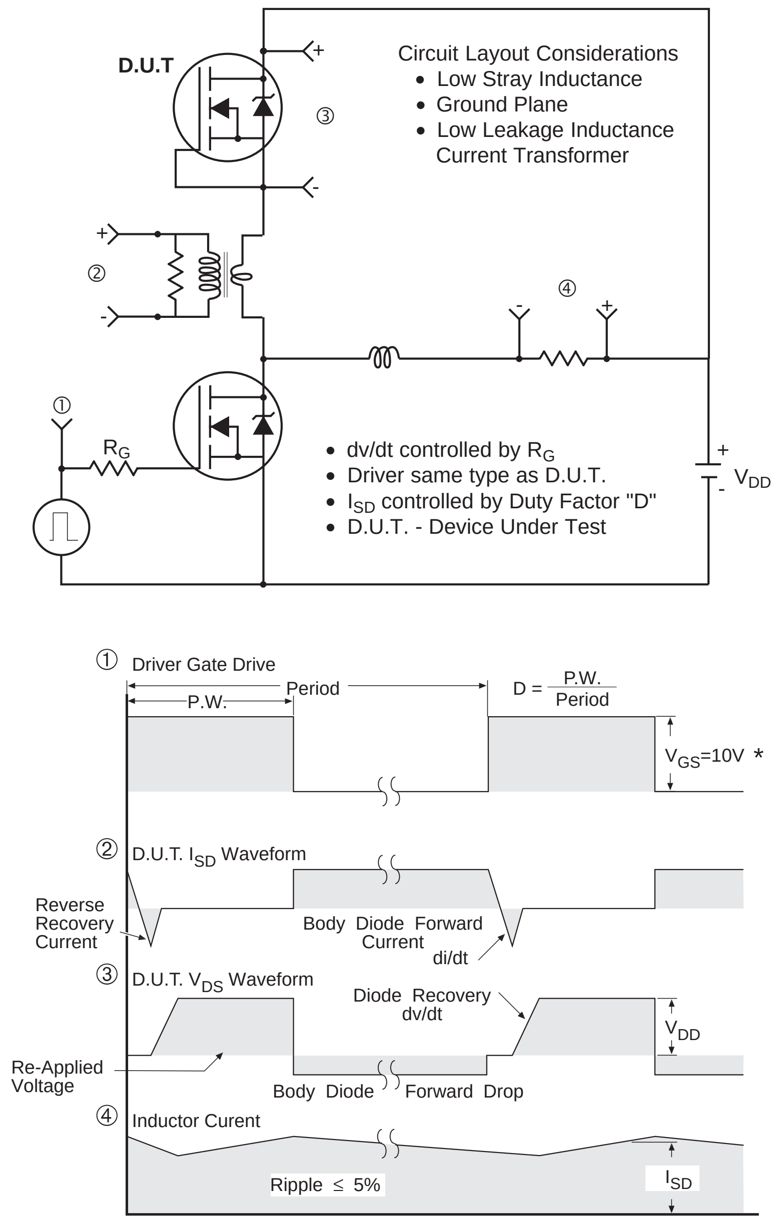


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

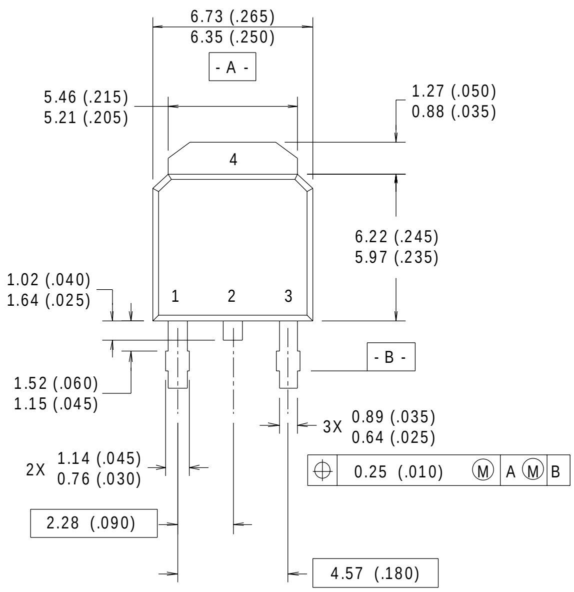


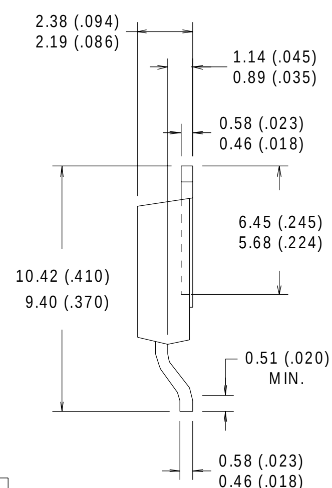
* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



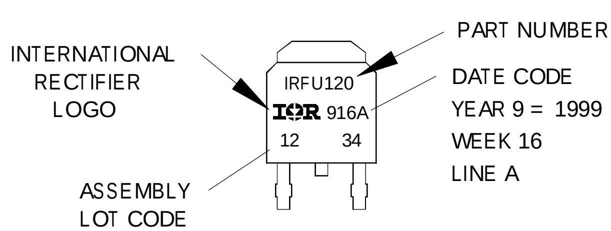


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

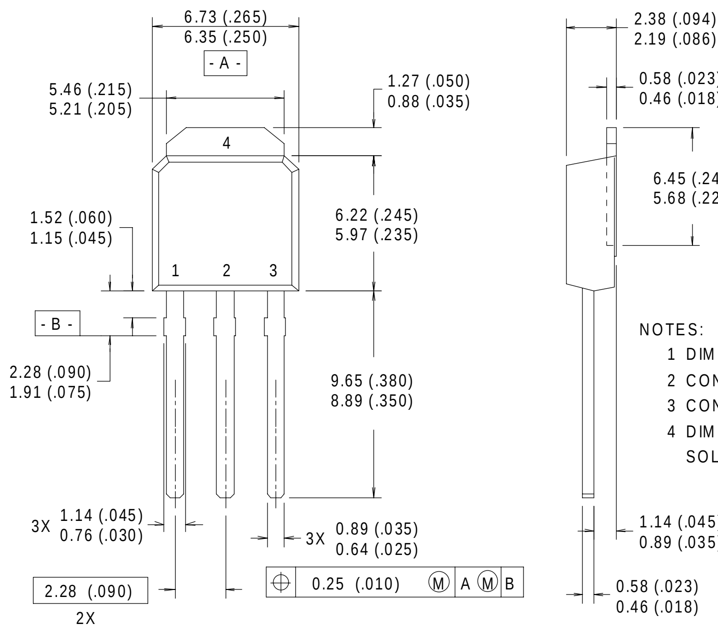
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

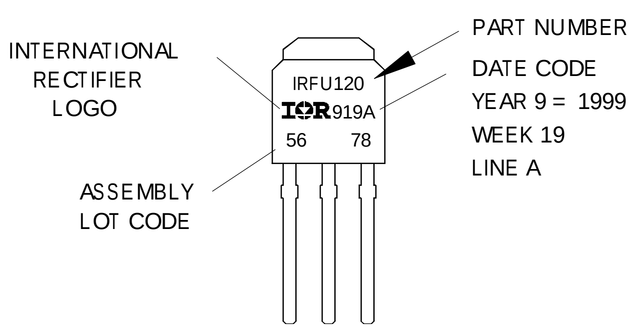


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

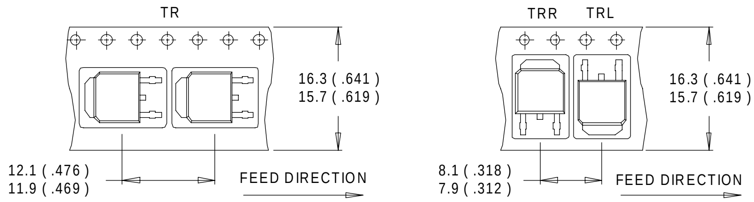
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

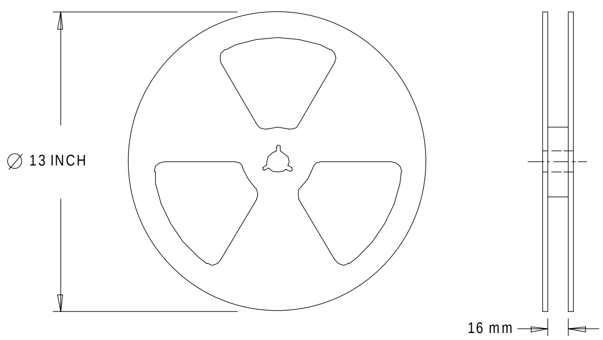


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 4.9mH $R_G = 25\Omega$, $I_{AS} = 10A$.

③ $I_{SD} \leq 10A$, $di/dt \leq 170A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

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