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Application Note AN4129

Green Current Mode PWM Controller FAN7601

1. Introduction

This application note describes the operation and features of the FAN7601. This device is a BCDMOS programmable frequency current mode PWM controller which is designed for off-line adapter applications and auxiliary power supplies. To reduce power loss at light and no load, the FAN7601 operates in burst mode and it includes a start-up switch to reduce the losses in the start-up circuit.
Because of the internal start-up switch and burst mode operation, it is possible to supply an output power of 0.5W with under 1W input power when the input line voltage is 265V. On no load condition, input power is under 0.3W.
The FAN7601 offers a latch protection pin for the protection of the system e.g. over voltage protection and/or thermal shutdown.
The internal over voltage protection function shuts down the IC operation when the supply voltage reaches 19V.
In addition, a soft start function is provided, and the soft start time can be varied. Figure 1 shows a block diagram for the FAN7601.
It contains the following blocks.

- Start-up circuit and reference
- Oscillator
- Soft start and latch
- Current sense and feed back
- Burst mode
- Output drive

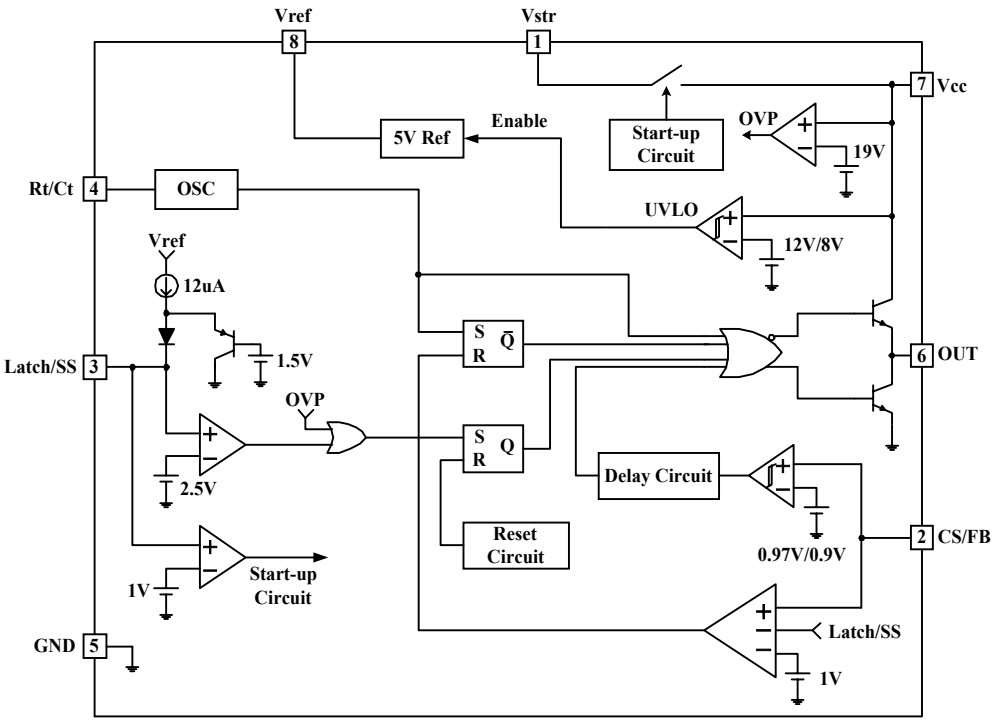


Figure 1. Internal Block Diagram of the FAN7601

2. Device Block Description

1. Start-up Circuit And Reference

The FAN7601 contains a start-up switch to reduce power loss in the external start-up circuit of conventional PWM converters. The internal start-up circuit charges the Vcc capacitor with a 1mA current source if the line is connected until the soft start is completed as shown in Fig. 2. The soft start function starts when the Vcc voltage reaches the start threshold voltage(typically 12V) and it ends when the LATCH/SS pin voltage reaches 1V. The internal start-up circuit starts charging the Vcc capacitor again if the Vcc voltage is lowered to the minimum operating voltage (typically 8V). In such a case the UVLO block shuts down the output drive circuit and some other blocks to reduce the IC current, and the soft start capacitor is discharged to zero voltage. If the Vcc voltage reaches the start threshold voltage, the IC starts switching again and the soft start capacitor is charged from zero voltage. The internal start-up circuit supplies
current until the soft start is completed .

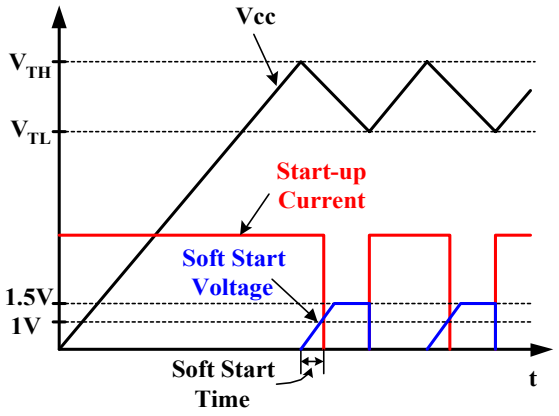


Figure 2. Start-up Current and Vcc Voltage

Figure 3 shows a typical start-up sequence for the FAN7601. The Vcc voltage should be higher than the minimum operating voltage at start-up to enter a steady state. If the Vcc voltage is higher than 19V, the over voltage protection function works. There is some delay in the over voltage protection circuit. The Vcc capacitor can be selected according to the soft start time and total gate charge(Qg) of the MOSFET. In the data sheet, the operating supply current is measured with a 1nF capacitor connected at the OUT pin. Therefore the real operating current necessary for the IC operation excluding the MOSFET drive is typically 2mA. During the soft start period (Tss), the Vcc capacitor is charged by a 1mA start-up current from the Vstr pin and the Vcc capacitor is discharged by a 2mA IC operating current and the MOSFET gate drive current. The MOSFET gate drive current is Qg×fsw. Qg increases according to the MOSFET drain source voltage, therefore the drive current is maximum when the input line voltage is highest. During the soft start period , the converter output voltage is very low, so few current is supplied to the Vcc capacitor from the Vcc winding. Therefore the Vcc capacitor must be large enough to supply sufficient current during the soft start time when starting up. The value of the Vcc capacitor is determined by (1) where 4V is the UVLO hysteresis and 2mA is the IC operating current and 1mA is the start-up current.

$$C_{Vcc} > \frac{Tss \cdot (2mA - 1mA + Q_g \cdot f_{sw})}{4V} \quad (1)$$

Figure 4 shows the Vcc voltage when starting up with a 47uF capacitor and a FQPF7N60 MOSFET. The input line voltage is 265V and the soft start time is about 40ms.

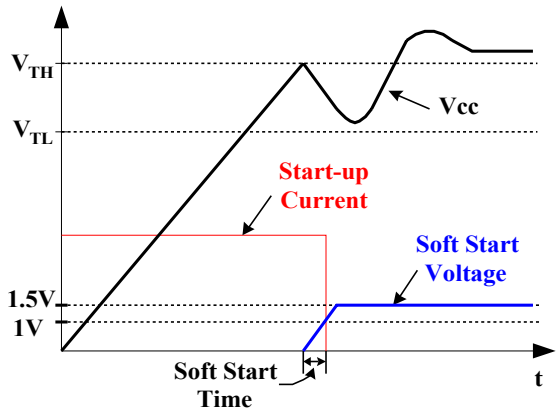


Figure 3. Typical Start-up Sequence for FAN7601

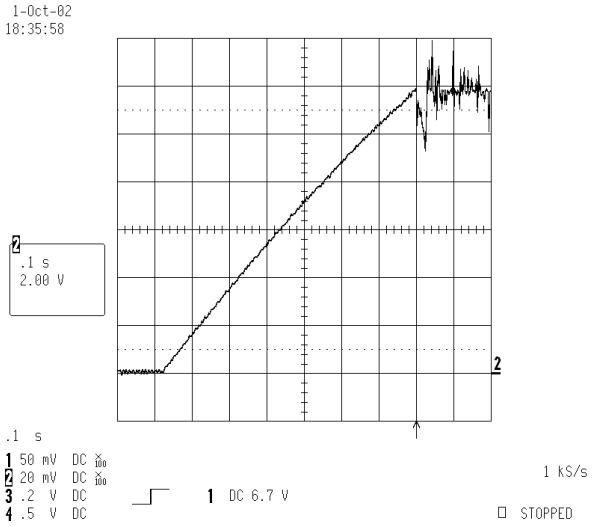


Figure 4. Vcc Voltage Waveform at Start-up

The FAN7601 provides the Vref pin. The reference output voltage is 5V. Because this voltage is the reference of the IC operation, a 100nF ceramic capacitor must be connected between the Vref pin and the GND pin to filter the switching noise as close as possible to the IC.

2. Oscillator

The oscillator frequency is programmed by selecting the values of Rt and Ct. The capacitor Ct is charged from the 5V reference through the resistor Rt to approximately 2.5V and discharged to 1.25V by an internal current sink. Figure 5 shows the oscillator frequency characteristics according to the variation of Rt and Ct. The values of Rt and Ct can be chosen with reference to Fig. 5.

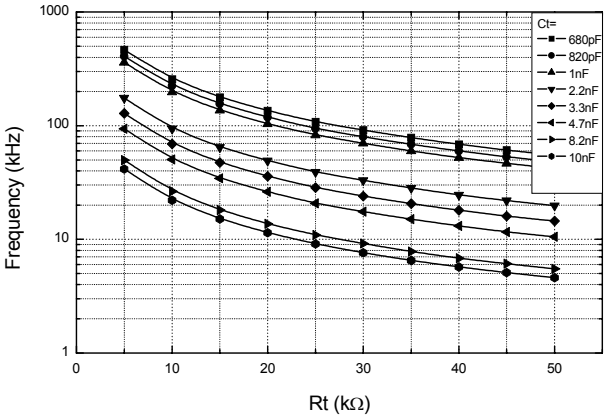


Figure 5. Oscillator Frequency Characteristics

3. Soft Start and Latch

The 12uA current source charges the soft start capacitor Css when the Vcc voltage reaches the start threshold voltage. The soft start ends when the Latch/SS pin voltage becomes 1V and the Latch/SS pin is charged up to 1.5V. The soft start capacitor is reset when the Vcc voltage is lower than the minimum operating voltage.
The soft start time Tss is calculated by (2).

$$Tss = Css/12\mu A \quad (2)$$

The latch protection is provided to protect the system.
The latch protection pin can be used for output over voltage protection and/or thermal protection etc. If the Latch/SS pin voltage is made greater than 2.5V by the external circuit, then the IC is shut down. The latch protection is reset when the Vcc voltage is lower than 5V.
Figure 6 shows a thermal protection circuit which uses an NTC thermistor. As the temperature rises the resistance of the NTC drops so the base voltage of the PNP transistor drops. Then the PNP transistor turns on and charges the Css. When the Latch/SS pin voltage is higher than 2.5V, the IC goes to the shut down mode. The exact values of resistors and NTC must be selected by an experiment because the $V_{BE(sat)}$ of PNP
transistors and the leakage current of Css vary according to the temperature.

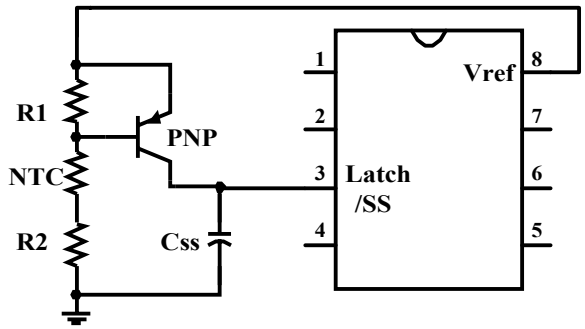


Figure 6. Thermal Protection Circuit

Figure 7 shows an output over voltage protection circuit. If the output voltage exceeds the sum of the zener diode voltage and the photo coupler forward voltage drop, then the capacitor Css is charged. In parallel with Css, a 1MΩ resistor is connected because of the leakage
current of the photo coupler. If a 1MΩ is not connected the leakage current of the photo coupler charges the Css up, and the latch protection operates abnormally.

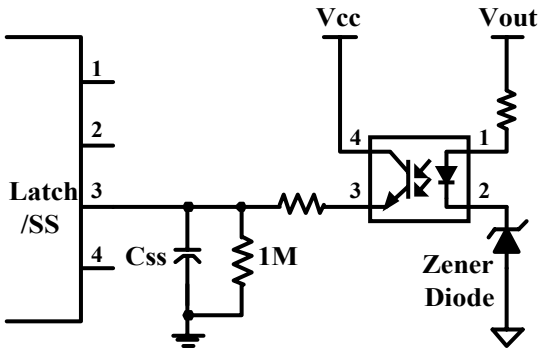


Figure 7. Output Over Voltage Protection Circuit

4. Current Sense and Feedback

The FAN7601 performs current sensing and output voltage feedback with only one pin. To achieve the two functions with one pin, an internal LEB(Leading Edge Blanking) circuit for filtering current sensing noise is not included because an external RC filter is necessary to add output voltage feedback and current sensing information.
Figure 8 shows the current sensing and feedback circuits. Rs is the current sensing resistor for sensing the switch current. The current sensing information is filtered by an RC filter composed of Rf and Cf. The current Ifb flowing through the photo transistor varies according to the feedback information and add an offset voltage on the sensed current information as shown in Fig. 8 and Fig. 9. When the CS/FB pin voltage touches 1V, the output drive circuit turns the MOSFET off. The higher the DC offset is, the shorter the switch-on time is. By varying the Ifb, the duty cycle is con-

trolled.

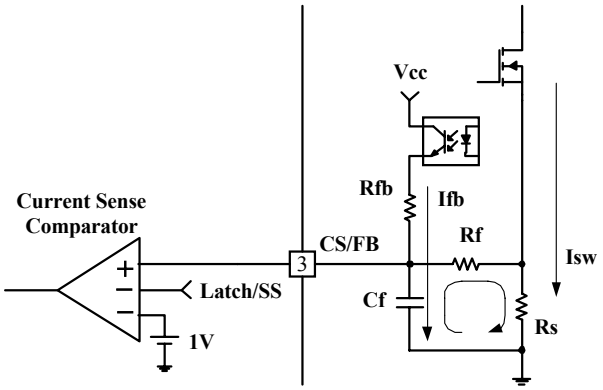


Figure 8. Current Sensing and Feedback Circuit

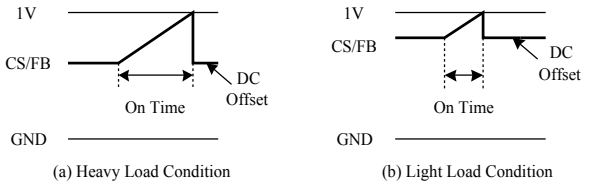


Figure 9. CS/FB Pin Voltage Waveforms

5. Burst Mode

The FAN7601 contains a burst mode block to reduce power loss at light and no load. A hysteresis comparator senses the CS/FB offset voltage for the burst mode. The FAN7601 enters burst mode when the offset voltage of the CS/FB pin is higher than 0.97V and exits the burst mode while the offset voltage is lower than 0.9V. The offset voltage is sensed during the switch-off time. In the burst mod block, there are about 4~8 switching cycles delay to filter the noise. By this burst mode, a power consumption of less than 1W can be achieved in standby mode.

6. Output Drive

The FAN7601 contains a single totem-pole output stage, designed specifically for a direct drive of a power MOSFET. The drive output is capable of up to 100mA peak current with typical rise and fall times of 45ns, 35ns respectively with a 1.0nF load. Additional circuitry has been added to keep the drive output in a sinking mode whenever the UVLO is active. This characteristic eliminates the need for an external gate pull-down resistor.
The output drive capability can be improved by adding one PNP bipolar transistor as shown in Fig. 10. In general, the on-resistance is high to prevent voltage spike at turn-on, only the turn-off characteristic is improved.

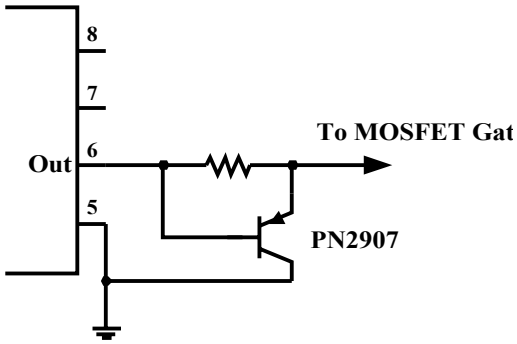


Figure 10. Circuit for Improving the Turn-Off Characteristic

3. Design Example

A 50W adapter is designed to illustrate the design procedure. The system parameters are as follows.

- Maximum output power(Po) : 50W
- Input voltage range : 85Vrms~265Vrms
- Output voltage(Vo) : 12.1V
- AC line frequency(fac) : 60Hz
- Adapter efficiency(η) : > 80%
- Switching frequency(fsw) : 91kHz

1. DC Link Capacitor and Bridge Diode

The DC link voltage becomes minimum when the output power is maximum and input line voltage is lowest. The minimum DC link voltage can be calculated using (3).

$$Vdc\_min = \sqrt{2 \cdot Vac\_min^2 - \frac{Po\_max}{\eta \cdot Cdc \cdot fac}} \quad (3)$$

If the minimum voltage is chosen then the capacitance can be calculated by (4).

$$Cdc > \frac{Po\_max}{\eta \cdot fac \cdot (2Vac\_min^2 - Vdc\_min^2)} \quad (4)$$

If we choose the minimum voltage to be 70% of the peak line voltage($\sqrt{2} \cdot 85V$) then Cdc must be larger than 142uF. The selected value is 150uF.
Figure 11 shows an experimental result for a 50W demo board with a 150uF capacitor. Because the measured efficiency is 84%, the minimum voltage is about 90V.

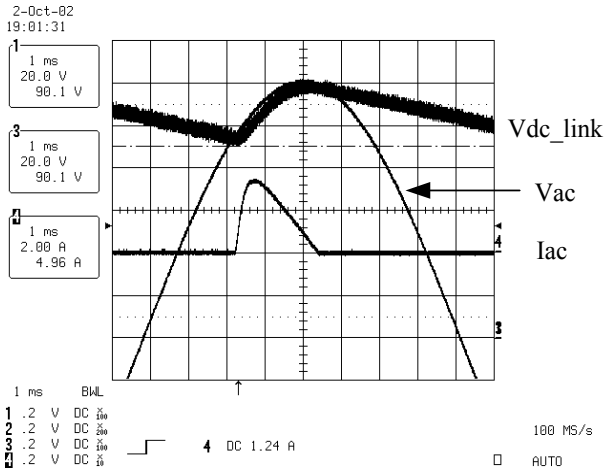


Figure 11. DC Link Voltage and Current Waveforms

The bridge diode conduction time can be calculated by (5) and the diode RMS current can be calculated by (6).

$$tc = \frac{1}{2\pi \cdot fac} \times \arccos\left(\frac{Vdc\_min}{\sqrt{2} \cdot Vac\_min}\right) \quad (5)$$

$$I_{BD(RMS)} = 2 \cdot (\sqrt{2} \cdot Vac\_min - Vdc\_min) \cdot Cdc \cdot \sqrt{\frac{2 \cdot fac}{3 \cdot tc}} \quad (6)$$

The calculated value is 1.3A and the selected bridge diode is KBP206(600V/2A).

2. Transformer Design

Since 2001, the European Commission has been regulating no load losses for AC adapters, battery chargers and external power supplies under 75W.
Table 1 shows the regulation target specification.

Table 1: European Commission Regulation Specification

Rated Input Power	No Load Power Consumption		
	Phase 1 1.1.2001	Phase 2 1.1.2003	Phase 3 1.1.2005
≥ 0.3W and < 15W	1.0W	0.75W	0.30W
≥ 15W and < 50W	1.0W	0.75W	0.50W
≥ 50W and < 75W	1.0W	0.75W	0.75W

At light and no load, the FAN7601 operates in burst mode to reduce the power loss. To meet the regulation specification the most important thing is to minimize the number of MOSFET switchings. The flyback converter transfers energy during the switch-off time. As the primary inductance of the flyback transformer increases, the energy transferred to the secondary side increases during one switching cycle. Therefore it is better to use a higher inductance transformer, but inductance is restricted by the size and cost of the transformer. In this design example, a 600uH transformer is selected and the ferrite core is EER2828. The transformer turns ratio is calculated when the input line voltage is lowest and the output power is maximum. The maximum duty ratio must be lower than 0.45 to prevent subharmonic oscillation. In this design example, the turns ratio must be higher than 0.174 by (7).

$$n > \frac{1 - D_{max}}{D_{max}} \cdot \frac{Vo + V_{Diode}}{Vdc\_min} \quad (7)$$

Once the minimum turns ratio is determined, then the numbers of primary and secondary turns is calculated when input line voltage is highest and the output power is maximum. If the converter operates in the CCM (Continuous Conduction Mode) then the turn-on time can be calculated by (8).

$$t_{on} = \frac{Vo + V_{Diode}}{n \cdot Vdc\_max + Vo + V_{Diode}} \cdot \frac{1}{fsw} \quad (8)$$

Then the number of primary turns can be obtained as in (9). Ae is the effective cross sectional area of the core and Bmax is the maximum flux density. Ae of EER2828 is 82.1mm^2 and Bmax is 0.15T. The calculated number of primary turns is 54. Then the number of secondary turns can be calculated by (10). The calculated number of secondary turns is 10. The air gap length can be calculated by (11).

$$Np = \left(\frac{Vdc\_max \cdot t_{on}}{Ae \cdot Bmax}\right) \quad (9)$$

$$Ns = Np\frac{Vo + V_{Diode}}{Vdc\_min} \cdot \frac{1 - D_{max}}{D_{max}} \quad (10)$$

$$lg = 4\pi \cdot 10^{-7} \cdot Ae \cdot \frac{N^2_P}{L} \quad (11)$$

If the primary inductance is not high enough, the converter can operate in the DCM(Discontinuous Conduction Mode) when the input line voltage is highest and the output power is maximum. For the DCM, the turn-on time can be calculated as in (12).

$$t_{on} = \frac{2 \cdot L \cdot Io \cdot n}{Vdc\_max} \quad (12)$$

Then the number of primary turns and secondary turns can be calculated by (9) and (10), respectively.
An adequate IC supply voltage is 12V considering the minimum operating voltage and the over voltage protection level. In this design example, the number of Vcc windings is selected so as to be the same as that of the secondary windings, namely 10 turns. If the number of windings is too small, the supply voltage can touch minimum operating voltage at no load; then the UVLO circuit comes into operation, increasing the power loss. If the number of windings is too large, the supply voltage can reach the over voltage protection level. If it proves difficult to prevent over voltage protection operation in normal mode, the circuit as shown in Fig. 12 is recommended for the Vcc circuit.

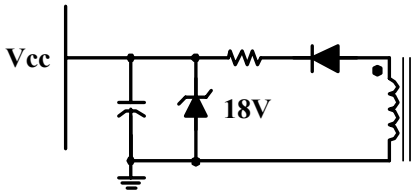


Figure 12. Zener Clamped Vcc Circuit

3. MOSFET Current Sensing Resistor Selection

Once the turns ratio of the transformer is determined, peak MOSFET current can be calculated. The sensed current information must be lower than 1V. If the resistance is too high, the output power can not be delivered because the MOSFET current is limited to the lower value.
The resistance can be determined as in (13). In this design example, a 0.5Ω resistor has been selected.

$$Rs < \frac{1}{\frac{Ns}{Np} \cdot \frac{Io}{1 - D_{max}} + \frac{Vdc\_min}{2 \cdot L} \cdot \frac{D_{max}}{fsw}} \quad (13)$$

4. Output Capacitor Design

The value of the output capacitor depends on the output voltage ripple and noise specification. In this design example two 1000uF capacitors are used.

5. MOSFET and Diode Selection

The current of MOSFET is highest when the input line voltage is lowest and the output power is at maximum.
The MOSFET RMS current can be approximated as in (14). The calculated value is 0.94A. A 600V, 2.7A(Tc=100°C) MOSFET FQPF7N60 has been selected.

$$I_{MOSFET(RMS)} \approx \frac{n \cdot Io}{1 - D_{max}} \sqrt{D_{max}} \quad (14)$$

The maximum average current of the output diode is the same as the maximum load current. In this case, 4.167A is the maximum load current. For better efficiency, two 100V, 20A schottky diodes are used. The diode is reverse biased when MOSFET is turned on. The reverse voltage depends on the MOSFET switching characteristic. If the MOSFET switching is fast, the diode junction capacitance and transformer leakage inductance resonate. Then the diode reverse voltage can exceed the diode rating. Therefore the MOSFET gate drive on resistance must be high enough to limit diode reverse voltage. Figure 13 shows the output diode voltage and MOSFET gate voltage waveforms when input line voltage is 265V and output power is 50W.
The gate drive on resistance is 75Ω. As shown in the figure, the diode reverse voltage exceeds the diode rating, 100V.
To reduce the diode reverse voltage, gate drive resistance is changed to 150Ω. Figure 14 shows the output diode voltage and MOSFET gate voltage waveforms with a 150Ω resistor. The diode reverse voltage is lowered because of MOSFET's slow turn-on characteristic.

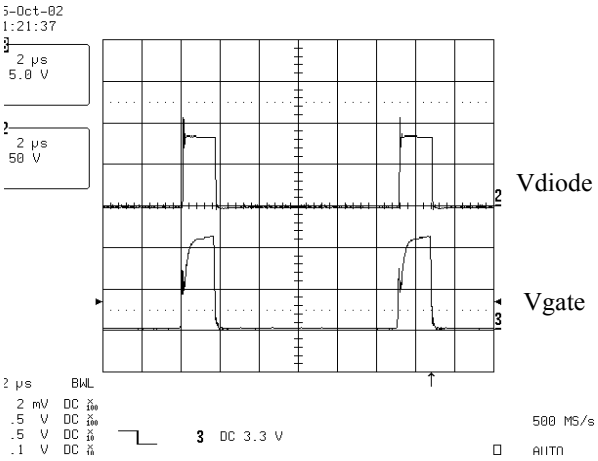


Figure 13. Diode Reverse Voltage and MOSFET Gate Voltage With 75Ω

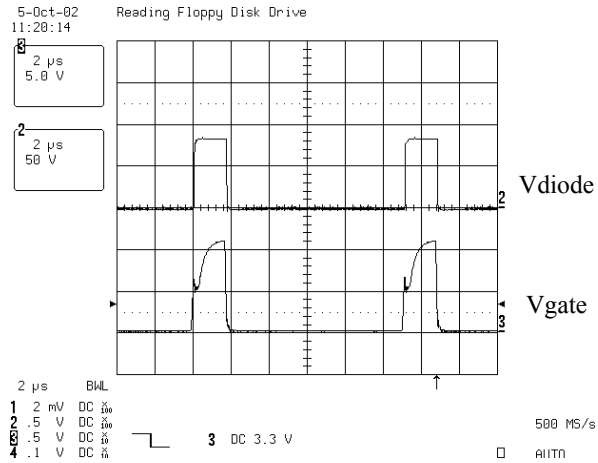


Figure 14. Diode Reverse Voltage and MOSFET Gate Voltage With 150Ω

6. Output Voltage Sensing Resistor and Feedback Loop Design

The output voltage sensing circuits cause power loss if the impedance is too low. The values of the output voltage sensing resistors are selected so that that power loss is under 10mW. The designed values are 27kΩ for the upper resistor and 7kΩ for the bottom resistor.

To control output voltage, a KA431 and an optocoupler are used as shown in Fig. 15. Equation (15) is the compensator transfer function. In this equation, k is the current transfer ratio of the optocoupler and this value is nonlinear.

$$\frac{V_{fb}}{V_O} = k \cdot \frac{R_f}{R3} \cdot \frac{1}{R_f \cdot C_f \cdot s + 1} \cdot \left(1 + \frac{1}{R1 \cdot C1 \cdot s}\right) \quad (15)$$

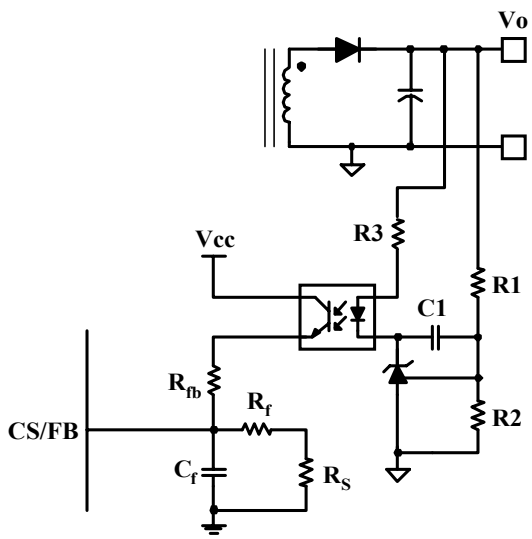


Figure 15. Output Voltage Compensation Circuit

The FAN7601 does not contain an LEB(Leading Edge Blanking) circuit, but the parasitic capacitance and resistance of the internal circuit work as an RC filter which filters switching noise. The parasitic capacitance is about 10pF and the parasitic resistance is about 20kΩ. These values are sufficient to filter switching noise; therefore a small capacitor can be used for C_f. The value of Rf should be 1000~2000 times higher than that of Rs. The filter resistor R_f causes some sensing delay so that the peak value of the filtered information is less than that of the real current information. The higher resistance causes a greater difference as shown in Fig. 16. The black line is the CS/FB voltage and the red and blue lines are the real current waveforms before filtering . The red line is the current waveform when the resistance is low and the blue line is the current waveform when the resistance is high. Because the current peak of the blue line is higher than that of the red line, more energy is transferred to the secondary side. Therefore standby power is lower with the higher resistance. But if the resistance is too high, the system can become unstable. The selected values are 10pF for C_f and 1kΩ for R_f .

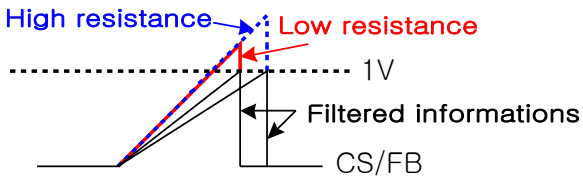


Figure 16. Current Sense Waveforms

For the stability of the system, capacitor C1 must be high enough. C1 can be selected as in (16). The selected value is 1nF.

$$C1 > \frac{10}{fsw} \cdot \frac{1}{2\pi \cdot R1} \quad (16)$$

R3 determines the control loop gain. If the value is too low, the system can become unstable. And if the value is too high, the output voltage regulation characteristics may be poor. The selected value is 1.5kΩ. If the value of R_{fb} is too high then the output voltage is not regulated at no load because the offset voltage of the CS/FB pin is lower than necessary. If the value is too low the audible noise increases. Because the current transfer ratio of the photocoupler is nonlinear, the value of R_{fb} has to be selected by experiment at no load. The selected value is 3.9kΩ.

7. Transformer Audible Noise

Because the FAN7601 operates in burst mode at light load and no load, it has a switching period and a non-switching period. Figure 17 shows the gate and output voltage at no load. Burst operation frequency is about 114Hz. The burst operation frequency varies according to load condition and the frequency is in the range of the audible frequency. Therefore the transformer may generate audible noise. The audible noise level depends on the control loop characteristic. If the loop speed is fast, audible noise increases but power loss decreases. If the loop speed is slow, audible noise decreases but power loss increases. There has to be a compromise between power loss and audible noise. Varnishing the transformer helps in reducing audible noise.

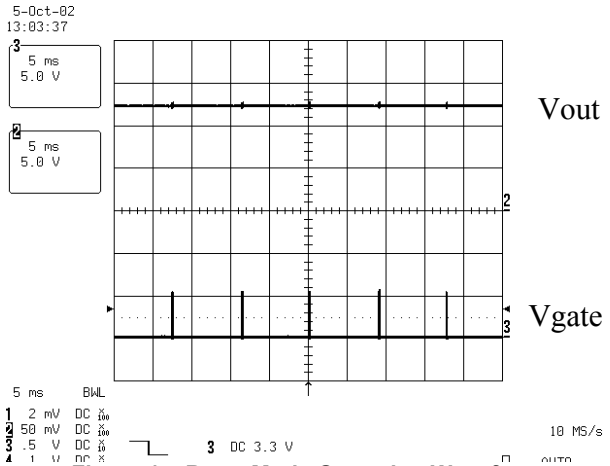


Figure 17. Burst Mode Operation Waveforms

8. How to Reduce Standby Power

1) Make the transformer inductance sufficiently high .
2) Make the control loop speed fast.
3) Use a higher resistor for R_f. But too high resistance makes the system unstable.

9. Slope Compensation

To prevent subharmonic oscillation when the duty ratio is greater than 0.5 for CCM, the slope compensation is necessary. Figure 18 shows the slope compensation circuit.

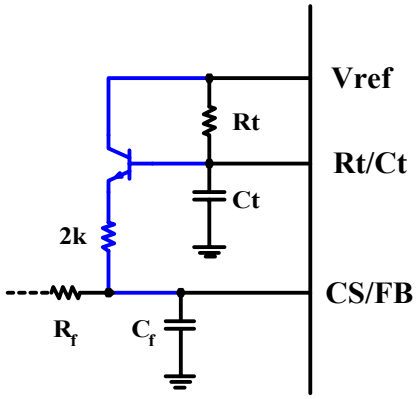


Figure 18. Slope Compensation Circuit

Figure 19 shows the designed application circuit diagram, table 2 shows the test results and table 3 shows the 50W adapter demo board components list. As can be seen in the table, the input power is less than 0.3W in the whole input voltage range at no load. The power was measured with a power meter from Voltech, PM3000.

10. On/Off Control

The Latch/SS pin can be used for the On/Off control with an NPN transistor. Figure 19 shows the On/Off control circuit.

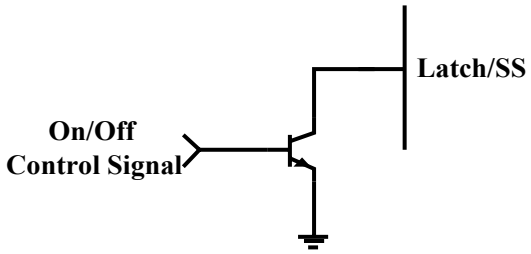


Figure 19. On/Off Control Circuit

Table 2: Experimental Results

	Input Power				
Output Power	85Vac	110Vac	220Vac	240Vac	265Vac
No Load	0.129W	0.136W	0.220W	0.245W	0.252W
0.5W	0.687W	0.703W	0.783W	0.796W	0.878W
50W	59.2W	58W	57.8W	57.6W	57.8W

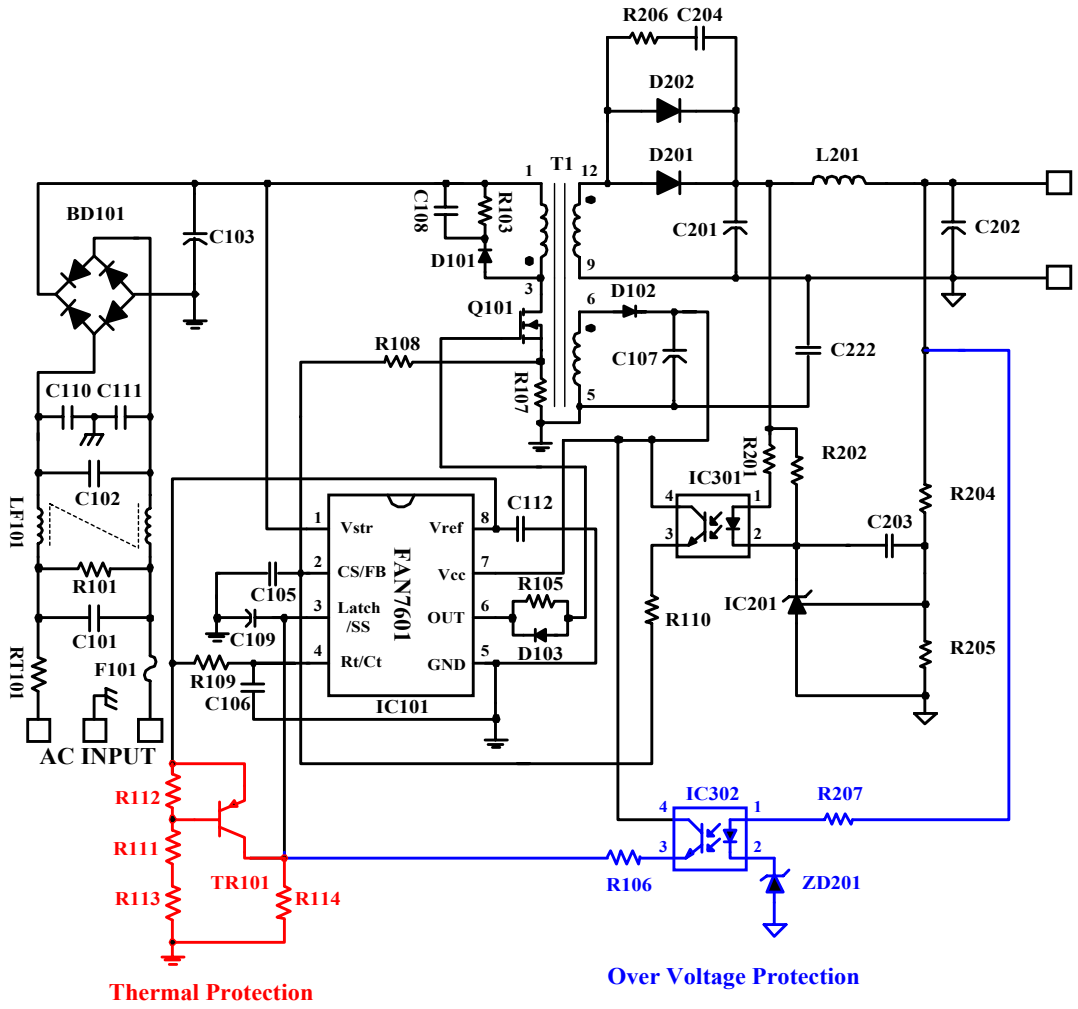
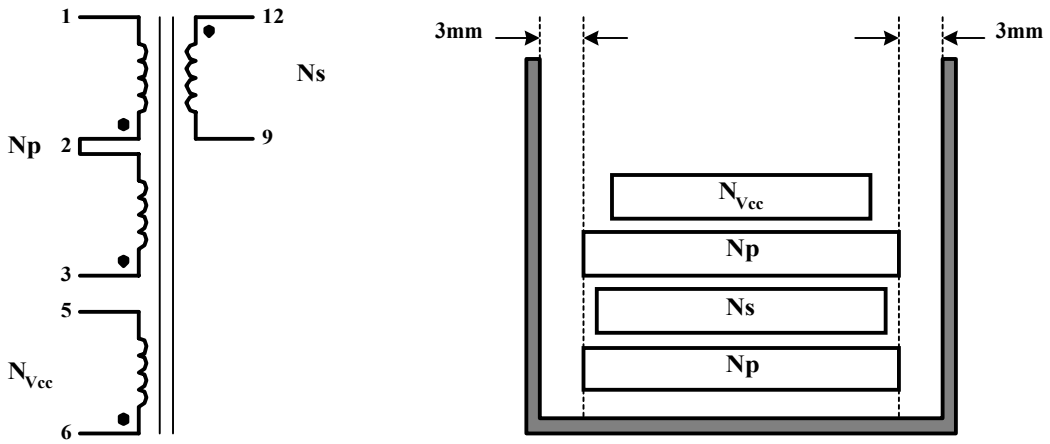


Figure 20. Application Circuit Diagram

Table 3: 50W Adapter Demo Board Part List

PART#	VALUE	NOTE	PART#	VALUE	NOTE
FUSE			CAPACITOR		
F101	250V 1A	-	C101	220nF/275V	Box Cap.
NTC			C102	100nF/275V	Box Cap.
RT101	5D-9	-	C103	150uF/400V	Electrolytic
R111	8k	-	C105	10pF	Ceramic
RESISTOR			C106	272	Miler
R101	-	-	C107	47uF/25V	Electrolytic
R103	56k	1/2W	C108	103	Film
R105	150	-	C109	0.47uF	Electrolytic
R106	10k	-	C110, 111	102/1kV	Ceramic
R107	0.5	1/2W	C112	104	Ceramic
R108	1k	-	C201, 202	1000uF/25V	Electrolytic
R109	8k	-	C203	102	Ceramic
R110	3.9k	-	C222	222/1kV	Ceramic
R112	1k	-	MOSFET		
R113	36k	-	Q101	FQPF7N60	Fairchild
R114	1M	-	INDUCTOR		
R201	1.5k	-	LF101	23mH	-
R202	1.2k	-	L201	9uH	-
R203	0	-	DIODE		
R204	27k	-	D101,102	UF4007	-
R205	7k	-	D103	1N4148	-
R206	10	1/2W	D202, 204	MBRF20100CT	-
R207	10k	-	ZD201	15V Zener/1W	-
IC			BD101	KBP206	-
IC101	FAN7601	Fairchild	TRANSISTOR		
IC201	KA431	Fairchild	TR101	2N3906	Fairchild
IC301, 302	H11A817B	Fairchild			

4. Transformer Specification



Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
N_P	1 → 2	0.35φ × 2	27	
N_S	9 → 12	0.65φ × 3	10	
N_P	2 → 3	0.35φ × 2	27	
N_{VCC}	5 → 6	0.2φ × 1	10	

Electrical Specification

	Pin	Value	Remarks
Inductance	1 - 3	600uH	100kHz, 1V
Leakage	1 - 3	15uH	2^{nd} shorted

Core

EER2828

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