HD49741NT, HD49733NT

Servo Controller

Description

The Hitachi HD49741NT/HD49733NT servo LSI for video tape recorders features an on-chip digital servo function for the drum motor and capstan motor, as well as an analog amplifier system, for wide-ranging applications on a variety of video tape recorder models. Available in a 56-pin shrink DIP package, HD49741NT/HD49733NT provides serial control connections with the system controller (microcomputer). This provides full servo LSI functions and means fewer peripheral components and connections are required.

Features

- Conforms to both PAL and NTSC standards.
- In conjunction with set function, mask ROM options allow setting of CFG (capstan frequency), DFG (drum frequency, search speed, etc.
- All VISS (VHS index search system) included on chip, with rewriting also possible.
- Search and output also available for VASS (VHS address search system), so operation in combination with microcomputer provides a full range of functions.
- CMOS analog technology provides on-chip CFG, DFG, PG (pulse generator), and CTLP (control pulse) amplifier, as well as adder amplifier loop f-characteristics, and analog switching for gain correction.
- Serial control used by microcomputer interface, so the system requires fewer connections.

Functional Description

DAC output using switched capacitor

Drum, capstan PD (phase detect), and FV (frequency voltage) conversion output is performed using switched capacitor technology for output of DC voltage. This means that, unlike conventional PWM output, a carrier elimination filter is not required. See Appendix B on SCF for further details.

70 different search speed variations on a single chip

Search speed is set using the mask ROM options. 14 speeds each for the SP, LP and EP modes in a NTSC system, as well as 14 modes each for the LP and LP modes in a PAL system are provided for a total of possible search speed settings. For further details, see serial control codes in On-chip Functions, and Mask ROM Options.

Six head angle settings

The head switch position is determined according to the PG mono-multi from the drum PG pulse. However, when the video head and audio head positions are different (when the video head is 4-head orthogonal/4-head double azimuth, the audio head is normally at a different position), a SW30 signal position (which indicates a fixed angle head switch position) is required for the head switch position created by the PG mono-multi. HD49741NT/HD49733NT allows six angle setting options for SW30 signals, for audio, video, and extra (extra head can be used for moving head, flying erase, etc.) heads. For further details, see serial control codes in On-chip Functions, Mask ROMs, and Timing Chart.

10 fine slow speed settings
Fine slow is made possible by intermittent tape transport, which is performed as illustrated below.

During fine slow, the speed of the capstan is controlled during the period from the point following the advance up to reverse advance in order to eliminate noise and to correct picture distortion. HD49741NT/HD49733NT allows serial control to be used to set this speed.

7-bit serial data and CR mono-multi setting of X-value correction
X-value correction (control pulse position correction) can be performed using serial control (Pin 5 CTL MM) or by altering the CR mono-multi time constant. For details, see Pin Functions and On-chip Functions.

7-bit serial data setting of tracking
Tracking can be controlled using serial control. For details, see On-chip Functions.

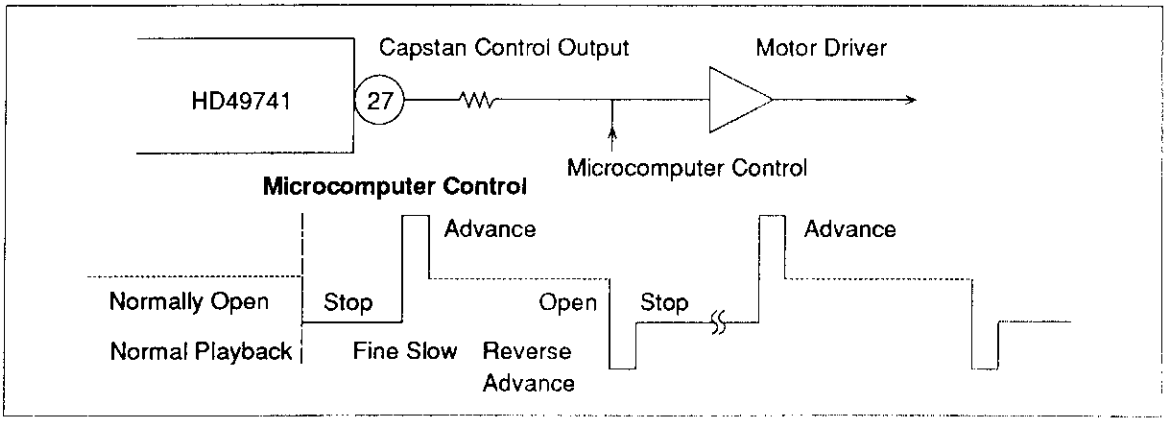
Supplementary V-pulse position delay (position) and shift settable using serial data
The delay time from the V-head switch edge to the supplementary V-pulse differs according to the special playback mode, which uses SW30 as a reference. HD49741NT/HD49733NT allows setting of this delay time (VP position) with the input of serial data. Serial data input can also be used to control the shift required during fine slow between the supplementary V-pulse position during acceleration (frame-by-frame) and the V-pulse position in the stop state. For details, see On-chip Functions.

Selection between f_{sc} and $3f_{sc}$ using serial data
The master clock of HD49741NT/HD49733NT is capable of using either f_{sc} or $3f_{sc}$. In the case of an f_{sc} master clock, crosstalk tends to be generated because f_{sc} enters the luminance FM band, while $3f_{sc}$ suppresses crosstalk generation. For details, see On-chip Functions.

Cross-over color distortion minimized by f_H correction using H-sync discrete integration
The drum speed system requires f_H correction to correct the H-cycle changes that occur in the special playback mode. HD49741NT/HD49733NT includes an f_H correction function that constantly monitors and corrects the H-sync cycle, so correction during startup of special playback minimizes cross-over color distortion and horizontal distortion. For details, see On-chip Functions.

Noise and no-H sync detection output for screen blackout
HD49741NT/HD49733NT counts the number of pulses in the H-sync frame, as well as the number of noise pulses within 1H period to provide output when the electric field strength is approximately below 4.0 to 4.5dBμ. This output is produced at the mode pin, and can be used for screen black-out when receiving channels for which there is no broadcast, etc. For details, see On-chip Functions.

Frame servo function
With VHS, recording and playback are performed with the CH1 head in the odd mode, and the CH2 in the even mode, though some manufacturers have



chosen to ignore this convention recently. HD49741NT/HD49733NT performs recording while precisely differentiating between these two modes, so the odd-even relationship is maintained for assembled recordings. During playback, beautiful assemblies are possible because the mis-aligned V signals instantaneously generated during playback are eliminated.

Supplementary V-pulse settable to H-OSC 3-value output or 2-pin output (HD49741NT)
Supplementary V-pulse is traditionally added immediately before the video V-pulse to protect against malfunction caused by noise. This method, however, generates mis-aligned V signals during special playback, can causes the playback screen to drop. HD49741NT/HD49733NT provides the V-pulse correction illustrated below.

This provides a choice of supplementary V-pulse signals: 3-value output (Pin 48) with sync level, pedestal level, and unsupplemented level; and 2-value output (Pin 48 and Pin 49). Note that the 2-pin output is available with HD49741NT only. For details, see On-chip Functions.

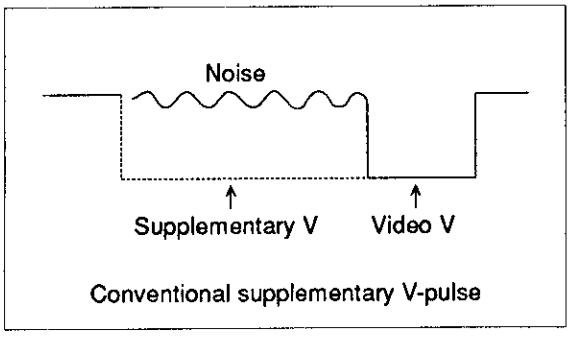
3 head switch outputs: Video-FF, audio-FF, extra-FF
Besides video and audio-FF, HD49741NT/HD49733NT includes extra-FF output designed for moving head and flying erase. FF angles are set using the mask ROM options for each head (note there is no extra head FF with HD49733NT). For details on head angle and head switching, see serial control codes in On-chip Functions, and Mask ROM Options.

On-chip V-sync separator circuit
HD49741NT/HD49733NT performs V-sync separation up/down counting the H-sync pulse input at the CMP-SYNC pin (Pin 50), so an external low-pass filter is not required.

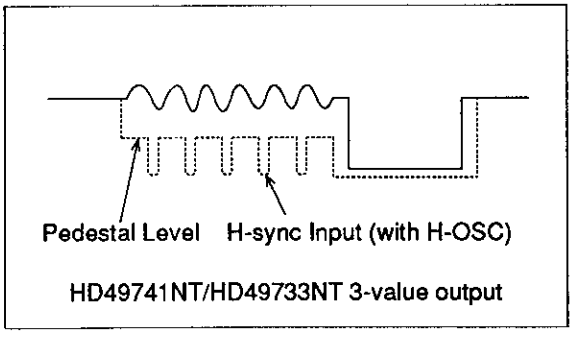
Analog signal input received by Schmitt circuit for rejection of other digital noise
HD49741NT/HD49733NT features on-chip DFG, CFG, PG, and DTLP input amplifiers with a Schmitt circuit for the elimination of small noise. Also, input of a pulse is followed by a preset period for digital processing, during which further input is cutoff, protecting against the invasion of noise between signals.

External synchronization input
With VTRs using frame memory, it is necessary to synchronize the reference frame signal of the frame memory controller (which is a signal equivalent to that of REF-30 of the servo IC) with REF-30 of the servo IC. HD49741NT/HD49733NT supports this type of synchronization. REF-30 (Pin 44) should be used when synchronization of the frame memory controller is necessary. Note that the pins used with HD49741NT are different from those used with HD49733NT. For details, see On-chip Functions.

CFG and CTLP output for SP/LP/EP discrimination
HD49741NT/HD49733NT does not include an on-chip SP/LP/EP discrimination function, but outputs CFG and CTLP so the microcomputer can perform such discrimination. Even during search operations, output signals are generated by counting down the CFG and CTLP pulses in accordance with the search speed, resulting in a constant pulse cycle. For details, see On-chip Functions.



Conventional supplementary V-pulse



HD49741NT/HD49733NT 3-value output

Non-linear PD output
With the drum and capstan PD function, 2-level detection output is required, with a large output gain for large errors, and small output during normal conditions. This is to allow both quick phase synchronization when a phase detection error occurs, and stability during normal conditions. HD49741NT/HD49733NT include these detection characteristics on-chip, so there is no need to attach the external non-linear circuitry required in the past.

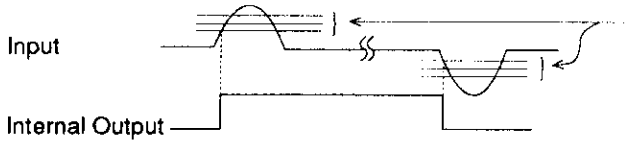
VISS discrimination capability even at more than 200X speed search
HD49741NT/HD49733NT performs VISS discrimination by pulse counting CTLP duty. A high-speed count clock allows detection of the VISS signal even in a 200X speed search mode.

On-chip waveform blunting, CTL, duty rewriting
For VISS rewriting, it is necessary to blunt the CTLP rise in order to protect against damage to the previously written CTLP signal. HD49741NT/HD49733NT apply CMOS analog technology to create an on-chip blunting circuit, so fewer external VISS functions are required.

On-chip automatic writing and discrimination of VISS code
VISS writing is performed automatically under serial control, with the blunting circuit operational during playback but not during recording. During playback, Pin 40 becomes LOW to indicate that VISS is detected.

CTLP amplifier with high f-characteristics, high gain, and fast rise at power ON
There is generally a problem with the rise speed of the CTLP amplifier at power ON. Since charge up time is required for external capacitance, however, the rise speed problem has generally been a hard to solve. HD49741NT/HD49733NT adopt a new type of circuitry is configured to eliminate the need for charge up, providing a quick-rise CTLP amplifier.

CTLP Schmitt input with three threshold levels
The Schmitt circuit of the CTLP amplifier allows stable operations over three switchable operation levels.



3-level threshold voltage switching performed automatically in accordance with SP, LP, EP, and search. Threshold level selection is performed automatically when the playback mode is set.

High-precision assemble

Assemble recording is performed using capstan phase control. Normally, the system is configured as illustrated below, but the improved precision of HD49741NT/HD49733NT allows use of a new system.

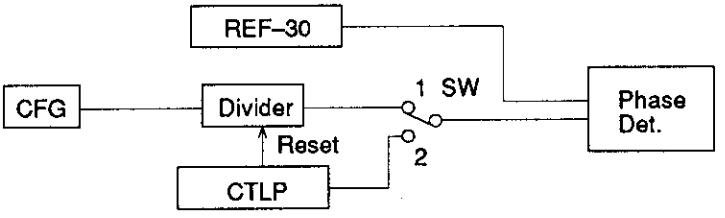
Fine slow CTLP Schmitt retrigger function

During fine slow, there are cases in the forward mode in which negative CTLP does not follow positive CTLP. To counteract this, HD49741NT/HD49733NT generate the subsequent CTLP signal automatically if the following pulse is not detected for approximately 10ms after the leading CTLP is entered.

Power ON reset without CTL head error current during full-rotating, half-rotating power ON

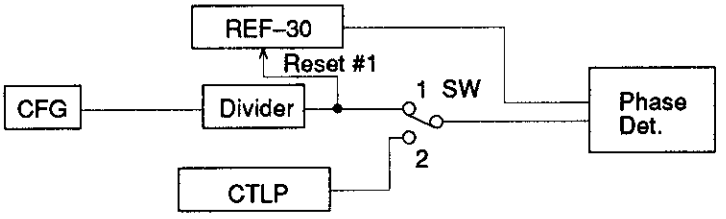
There are cases in which the tape is in its rotating status when the power of the VCR is OFF. HD49741NT/HD49733NT resets the CTL write circuit at power ON, no matter what the tape status, to protect against writing of the CTLP pulse. For details, see Pin Functions.

Normal System



For assemble recording, SW1 is switched in accordance with the status of SW2 (at this time, a divider reset is applied by CTLP) to enter the REC mode. At this time the reset is released.

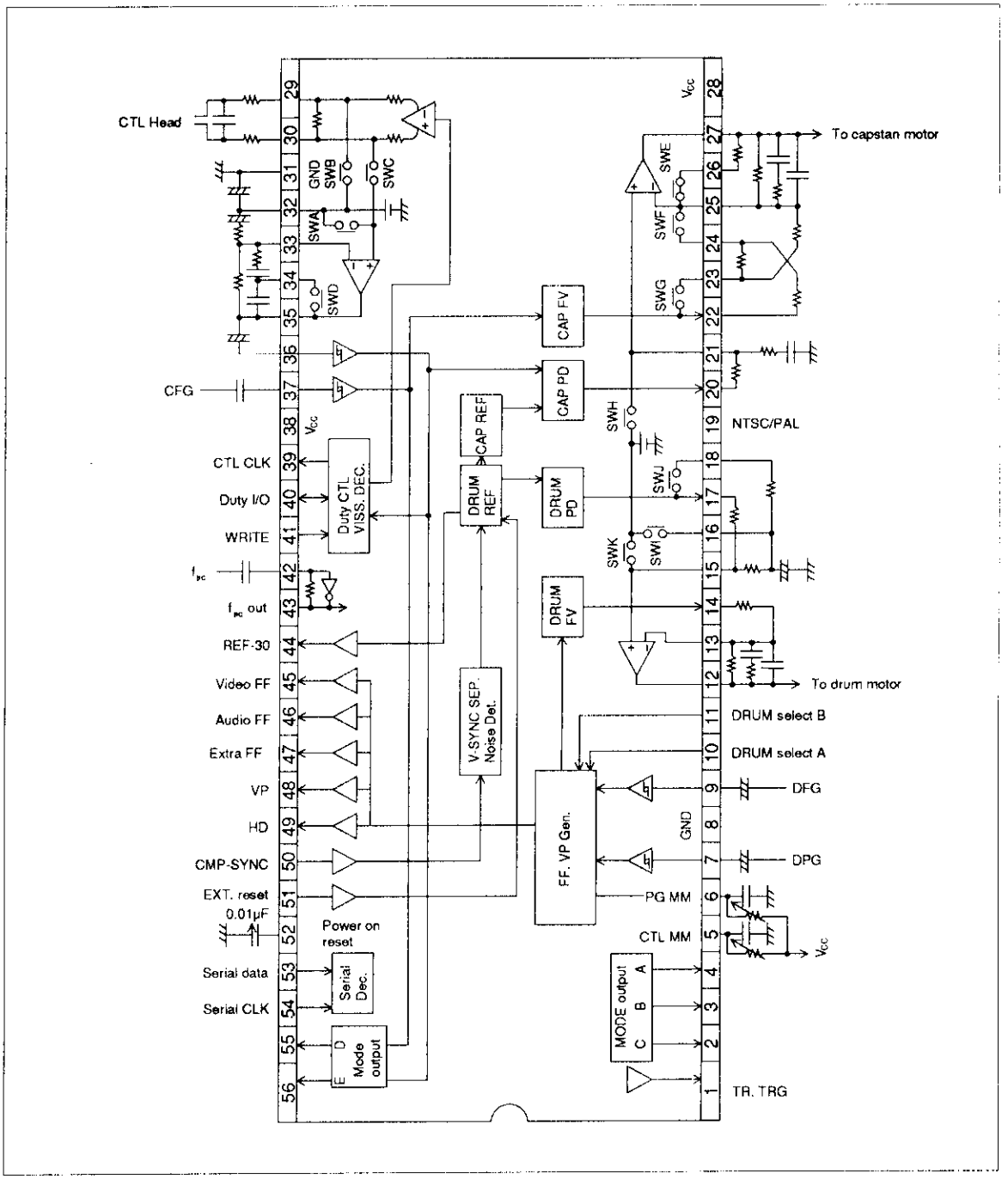
New HD49741NT/HD49733 System



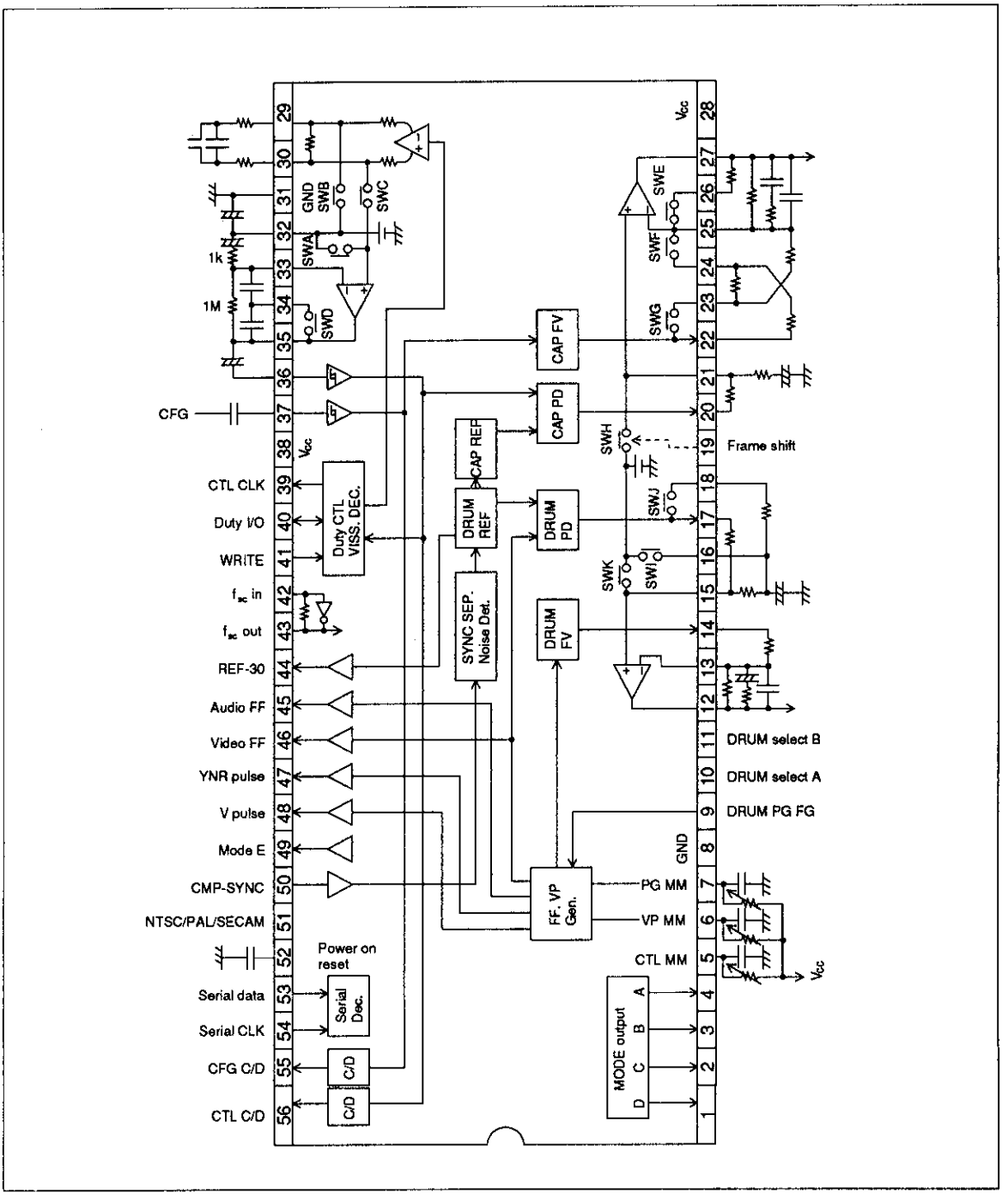
Single REF-30 reset applied at moment of switching of SW1 in accordance with the status of SW2

Block Diagram

HD49741NT Block Diagram and Pin Arrangement

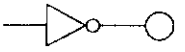
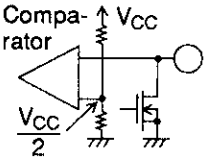


HD49733NT Block Diagram and Pin Arrangement

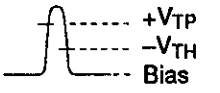
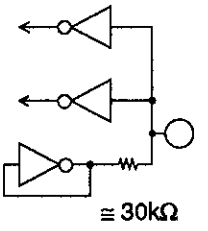
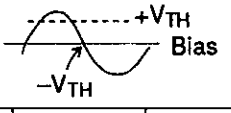
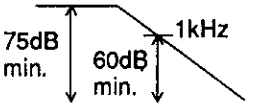


Pin Functions

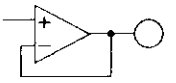
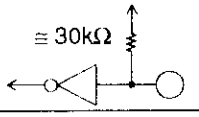
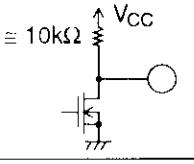
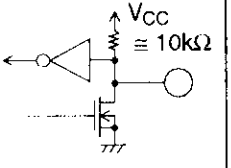
HD49741NT Pin Functions

Pin No.	Pin Name	Function				I/O Format
1	TRACKING TRIGGER					
2	MODE OUTPUT CAP PDS reference	bit 5 4 2 1 0	A	B	C	
3		0 0 1 1 1	SP	$\overline{SP}$	LP	
4		0 1 1 1 1	SP	EP	LP	
		1 0 1 1 1	CTL DELAY COUNTER	H-OSC	Noise Det.	
		1 1 1 1 1	CAP PD	DRUM FG	DRUM PG	
		See On-chip Functions. Refer to Time Chart for CTL delay counter Refer to H-OSC for H-OSC Refer to noise det for noise detection.				
5	CTL DELAY MM	Time constant: 1 to 40ms See Time Chart Retriggerable (discharge pulse = $4096/f_{sc}$)				
6	PG MM	Time constant: 0 to 60° DEG See Head SW Timing Non-retriggerable				

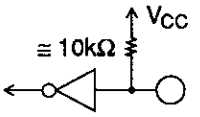
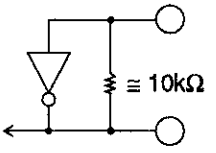
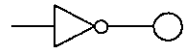
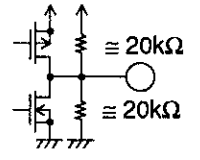
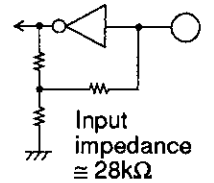
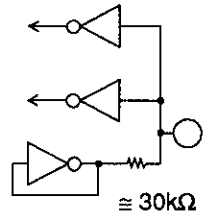
HD49741NT Pin Functions (cont)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>I/O Format</th></tr>
<tr><td>7</td><td>DRUM PG IN</td><td>Approximately 2V
Schmitt input/internal bias
See Head SW Timing
  </td><td rowspan="2"> 
* TEST is used for checking SP in the case of a double azimuth head set. When this mode is specified, HD49741NT/ HD49733NT recognizes SP mode tape as LP mode tape, and inverts the head selection switch to run in the SP mode.</td></tr>
<tr><td>9</td><td>DRUM FG IN</td><td>Approximately 2.5V
Schmitt input/internal bias
See Head SW Timing
  </td></tr>
<tr><td>10
11</td><td>DRUM select A</td><td>3-value input
Open = "M"
(1.9V to 3.1V)
See Head SW Timing
Different from selection format for HD49733.
<table><tr><th>B \ A</th><th>H</th><th>M</th><th>L</th></tr><tr><td>H</td><td>2Head ①</td><td>2Head ②</td><td>DA4-④</td></tr><tr><td>M</td><td>DA4-①</td><td>DA4-②</td><td>DA4-③</td></tr><tr><td>L</td><td>DA4 ① TEST*</td><td>DA4-② TEST*</td><td>DA4-③ TEST*</td></tr></table></td><td></td></tr>
<tr><td>21
23
24
25
26
27</td><td>CAPSTAN MIX Amp</td><td rowspan="2">• Open gain
• No oscillation during all feedback
 
• Output D range 0 to 5V (no load)
• Output impedance = 2kΩ max.</td><td rowspan="2"></td></tr>
<tr><td>12
13
15
16
18</td><td>DRUM MIX Amp</td></tr>
</table>

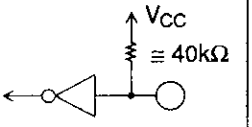
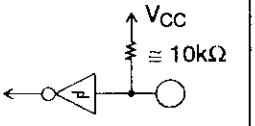
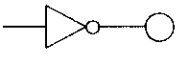
HD49741NT Pin Functions (cont)

Pin No.	Pin Name	Function			I/O Format
14 22	Drum FV out CAP FV out	Switched capacitor DA output Output D range = 0.5V max. to 4.3V min. Input impedance = 100Ω max.			
17 20	Drum PD out CAP PD out	Switched capacitor DA output Output D range = 0.5V max. to 4.3V min. Input impedance = 2Ω max.			
19	NTSC/PAL	2-value input open = "H"	H	NTSC	≅ 30kΩ 
			L	PAL	
29 30	CTL Head ⊖ CTL Head ⊕	I/O control head pin			
32 33 34 35	CTLP Amp	• Open gain • No oscillation during all feedback • Output D range 0 to 5V (no load) • Output impedance = 2kΩ max.	80dB min. 60dB min. 10kHz		
36	CTLP IN	Schmitt input V_{TH} 3-level switching Approximately 2.5V internal bias See CTL Schmitt V_{TH}	$+V_{TH}$ Bias $-V_{TH}$		
37	CFG IN	Same as DFG IN.			
39	CTL CLK	2-value output, pull up See VISS, VASS			≅ 10kΩ Vcc 
40	Duty I/O	2-value input/output, pull up See VISS, VASS	Input Duty Mode	Output VISS mode	Vcc ≅ 10kΩ 
			H	Duty = "0"	VISS non-detect
			L	Duty = "1"	VISS detect (latch)

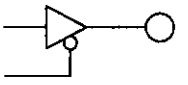
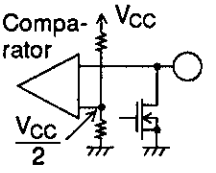
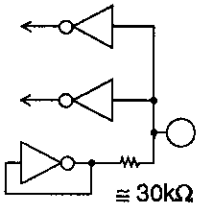
HD49741NT Pin Functions (cont)

Pin No.	Pin Name	Function			I/O Format
41	WRITE	2-value output, pull up See VISS, VASS	H	PB CTL, rewrite	
			L	Normal	
42 43	f_{sc} in $3f_{sc}$ out	Input sensitivity 150m V_{pp} min. (f_{sc}) 350m V_{pp} min. ($3f_{sc}$) With oscillator function See f_{sc} Input Circuit. For $f_{sc}/3f_{sc}$ switching, see Serial Data.			
44	REF 30	See Time Chart.			
45	VFF	See Head SW Timing.			
46	AFF	See Head SW Timing.			
47	EFF	See Head SW Timing.			
49	HD	See V-pulse Timing.			
48	V-pulse (VP)	See V-pulse.			
50	CMP SYNC	2-value input • Digital level input or analog capacitive coupling input.			
51	Ext. Reset	3-value input Open = "M" See External Synchronization			

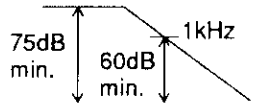
HD49741NT Pin Functions (cont)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>I/O Format</th></tr>
<tr><td>52</td><td>Power ON Reset</td><td>At power ON, reset performed to current does not flow to CTL head. Be sure to include 0.01µF between this pin and GND.</td><td> 
</td></tr>
<tr><td>53
54</td><td>Serial Data
Serial CLK</td><td>2-value input (Schmitt)
Pull up
See Serial Input.</td><td> 
</td></tr>
<tr><td>55
56</td><td>Mode output</td><td>
<table>
<tr><td>bit 3 2 1 0</td><td>D</td><td>E</td></tr>
<tr><td>0 1 1 1</td><td>CFG C/D</td><td>CTL C/D</td></tr>
<tr><td>1 1 1 1</td><td>CFG</td><td>CFG 30</td></tr>
</table>
CFG C/D: CFG counted down according to search speed and then is output.
CTL C/D: CTL counted down according to search speed and then is output.
CFG 30: During REC, CFG countdown 30Hz (25Hz for PAL), which indicates capstan phase comparison signal is output..
See 4. On-chip Functions, and Serial Data Table.
</td><td>  </td></tr>
<tr><td>8
31</td><td>GND</td><td>Ground</td><td></td></tr>
<tr><td>28
38</td><td>V_{CC}</td><td>Connected to V_{CC} supply</td><td></td></tr>
</table>

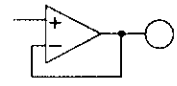
HD49733NT Pin Functions

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>I/O Format</th></tr>
<tr><td>1
2
3
4</td><td>Mode Output</td><td>See 4. On-chip Functions, and Serial Code table.</td><td> 
For SP, and $\overline{SP}$ mode output, high impedance and HIGH level.</td></tr>
<tr><td>5</td><td>CTL DELAY MM</td><td>Time constant: 1 to 40ms
See Time Chart
Retriggerable (discharge pulse = 4096/fsc)</td><td rowspan="3">  </td></tr>
<tr><td>6</td><td>VP MM</td><td>Time constant: 0 to 0.6ms
Non-retriggerable</td></tr>
<tr><td>7</td><td>PG MM</td><td>Time constant: 0 to 42° DEG
Non-retriggerable</td></tr>
<tr><td>9</td><td>DRUM PFG IN</td><td>3-value input, open = "M"</td><td rowspan="2"> 
* TEST is used for checking $\overline{SP}$ in the case of a double azimuth head set. When this mode is specified, HD49741NT/ HD49733NT recognize SP mode tape as LP mode tape, and inverts the head selection switch to run in the SP mode.</td></tr>
<tr><td>10
11</td><td>DRUM select A</td><td>3-value input
Open = "M"
(1.9V to 3.1V)
Different from selection format for HD49741.
<table>
<tr><th>B \ A</th><th>H</th><th>M</th><th>L</th></tr>
<tr><td>H</td><td>DA4 ①</td><td>2Head</td><td>4Head HiFi</td></tr>
<tr><td>M</td><td>DA4 ②</td><td>4Head</td><td>4Head HiFi</td></tr>
<tr><td>L</td><td>DA4 ② TEST</td><td>4Head TEST</td><td>4Head HiFi TEST</td></tr>
</table></td></tr>
</table>

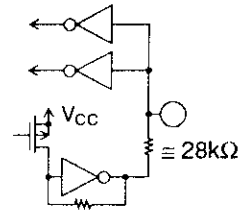
HD49733NT Pin Functions (cont)

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th><th>I/O Format</th></tr>
<tr><td>21
23
24
25
26
27</td><td>CAPSTAN
Mix Amp</td><td rowspan="2">• Open gain
• No oscillation during all feedback
• Output D range 0 to 5V (no load)
• Output impedance = 2kΩ max.
  </td><td rowspan="2"></td></tr>
<tr><td>12
13
15
16
18</td><td>DRUM
Mix Amp</td></tr>
<tr><td>14

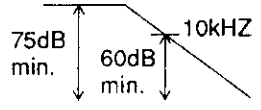
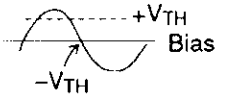
22</td><td>DRUM FV out

CAP FV out</td><td>Switched capacitor DA output
Output D range = 0.5V max. to 4.3V min.
Input impedance = 100Ω max.</td><td rowspan="2">  </td></tr>
<tr><td>17

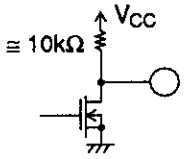
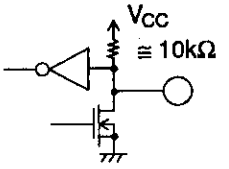
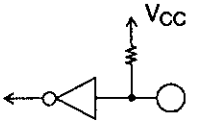
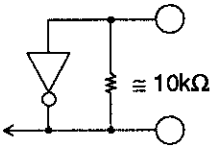
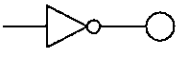
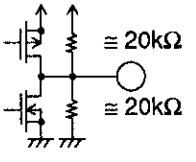
20</td><td>DRUM PD out

CAP PD out</td><td>Switched capacitor DA output
Output D range = 0.5V max. to 4.3V min.
Input impedance = 2Ω max.</td></tr>
<tr><td>19</td><td>FRAME SHIFT
(CAP PD Fix)</td><td>• Frame shift PD fix Tape speed 5% down During normal mode only
<table><tr><th></th><th>Out</th><th>In</th></tr><tr><td>H</td><td>—</td><td>FRAME SHIFT</td></tr><tr><td>M</td><td>Loop on</td><td>Loop on</td></tr><tr><td>L</td><td>PD Fix</td><td>PD Fix</td></tr></table></td><td>  </td></tr>
<tr><td>29

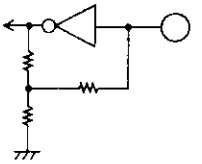
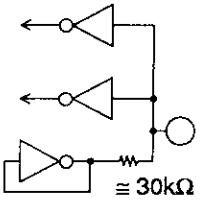
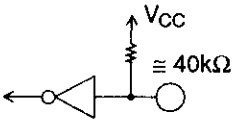
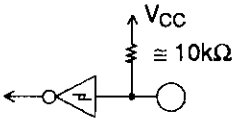
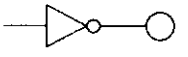
30</td><td>CTL Head

⊖ ⊕</td><td>I/O control head pin</td><td></td></tr>
<tr><td>32
33
34
35</td><td>CTLP Amp</td><td>• Open gain
• No oscillation during all feedback
• Output D range 0 to 5V (no load)
• Output impedance = 2kΩ max.
  </td><td></td></tr>
<tr><td>36</td><td>CTLP IN</td><td>Schmitt input V_{TH} 3-level switching
Approximately 2.5V internal bias
See CTL Schmitt V_{TH}</td><td></td></tr>
<tr><td>37</td><td>CFG IN</td><td>Schmitt input V_{TH}
approximately ±25mV
Approximately 2.5V internal
  </td><td></td></tr>
</table>

HD49733NT Pin Functions (cont)

Pin No.	Pin Name	Function	I/O Format
39	CTL CLK	2-value output, pull up	
40	Duty I/O	2-value input/output, pull up See on-chip functions VISS, VASS H: Input Duty Mode = Duty = "0", Output VISS mode = VISS non-detect L: Input Duty Mode = Duty = "1", Output VISS mode = VISS detect (latch)	
41	WRITE	2-value output, pull up See VISS, VASS H: PB CTL, rewrite L: Normal	
42 43	f_{sc} in $3f_{sc}$ out	Input sensitivity 150m V_{pp} min. (f_{sc}) 350m V_{pp} min. ($3f_{sc}$) With oscillator function See f_{sc} Input Circuit. For $f_{sc}/3f_{sc}$ switching, see Serial Data.	
44	REF 30	See Time Chart.	
45	Audio-FF	See Head SW Timing.	
46	Video-FF	See Head SW Timing.	
47	YNR-pulse	See On-chip Functions.	
49	Mode E	See On-chip Functions.	
48	V-pulse (VP)	See On-chip Functions.	

HD49733NT Pin Functions (cont)

Pin No.	Pin Name	Function	I/O Format
50	COMP SYNC	• 2-value input. Digital level input or analog capacitive coupling input.	 Input impedance 28Ω
51	NTSC/PAL/ SECAM	3-value input Open = "M" See External Synchronization H: NTSC M: PAL L: SECAM	 ≅ 30kΩ
52	Power ON Reset	At power ON, reset performed to current does not flow to CTL head. Be sure to include 0.01µF between this pin and GND.	 Vcc ≅ 40kΩ
53 54	Serial Data Serial CLK	2-value input (Schmitt) Pull up See On-chip Functions.	 Vcc ≅ 10kΩ
55	CFG C/D	CFG counts down search speed only and then is output.	
56	CTL C/D	CTL counts down search speed only and then is output.	
8 31	GND	Ground	
28 38	V_{CC}	Connected to V_{CC} supply	

Mask ROM Options

The mask ROM options available with the HD49741NT/HD49733NT are listed below. When ordering mask ROM options, fill in the necessary information in Appendix C Hitachi C-MOS Servo IC ROM Change Specifications, and consult with your Hitachi representative.

The first step is to select the base chip. Appendix A describes the differences between HD49741 and HD49733.

Once a selection is made between HD49741 and HD49733, select from among the five mask ROMs listed below. Generally, the selection of mask ROM options must be based on the mechanical configuration and heads used in the VCR.

CFG frequency
Defines the oscillation frequency of the capstan frequency generator (CFG).
Condition: NTSC SP mode frequency

DFG frequency
Defines the oscillation frequency of the head drum frequency generator (DFG).
Condition: NTSC normal record/playback mode frequency

Search speed
Uses integer to set up to 14 search speeds for each record mode.

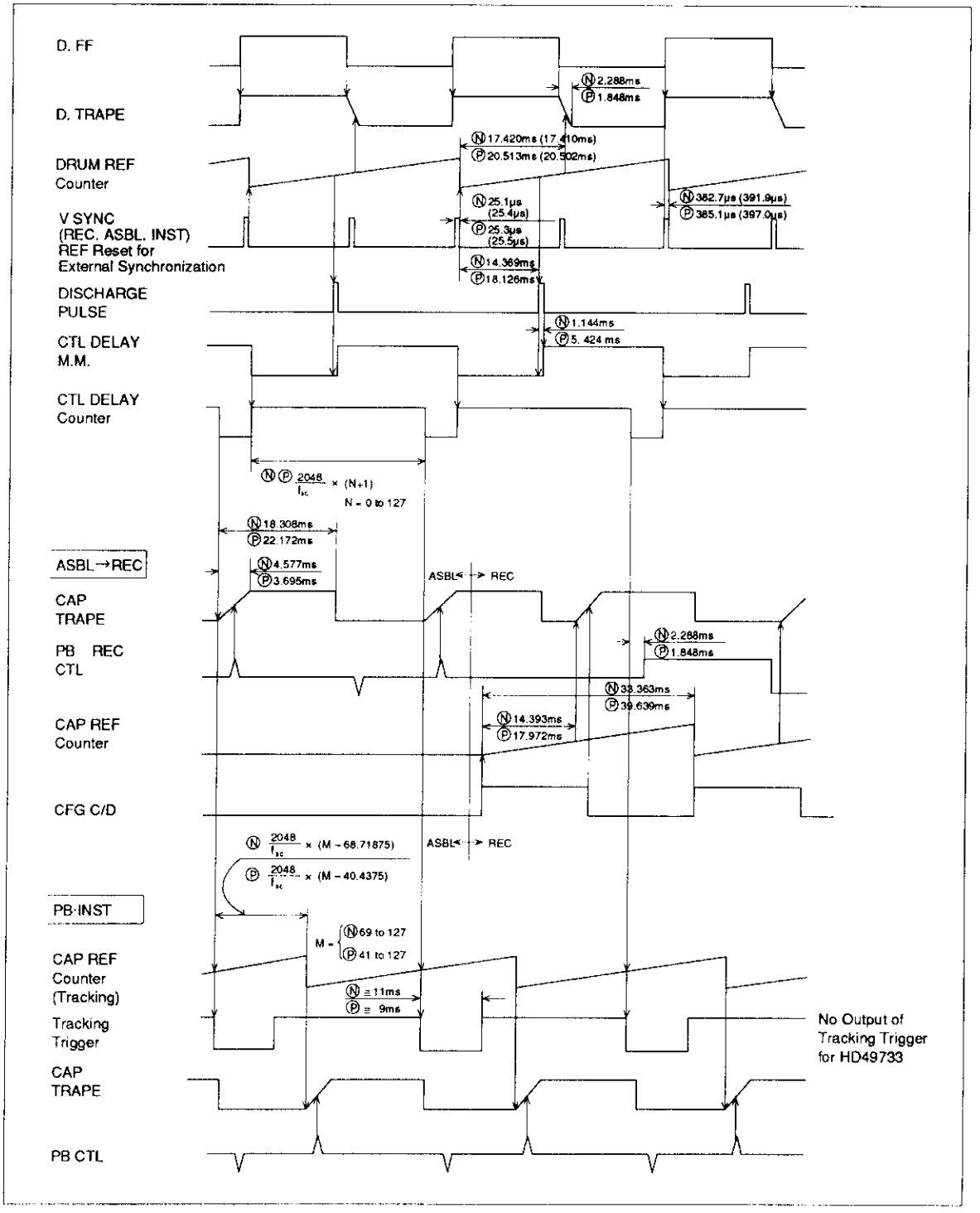
Head angle
Allows setting of up to six switching pulse signal angles for each of the heads: video head, audio head, extra head.

VP output polarity
Selects from among three VP signal pulse polarities.

Timing Charts

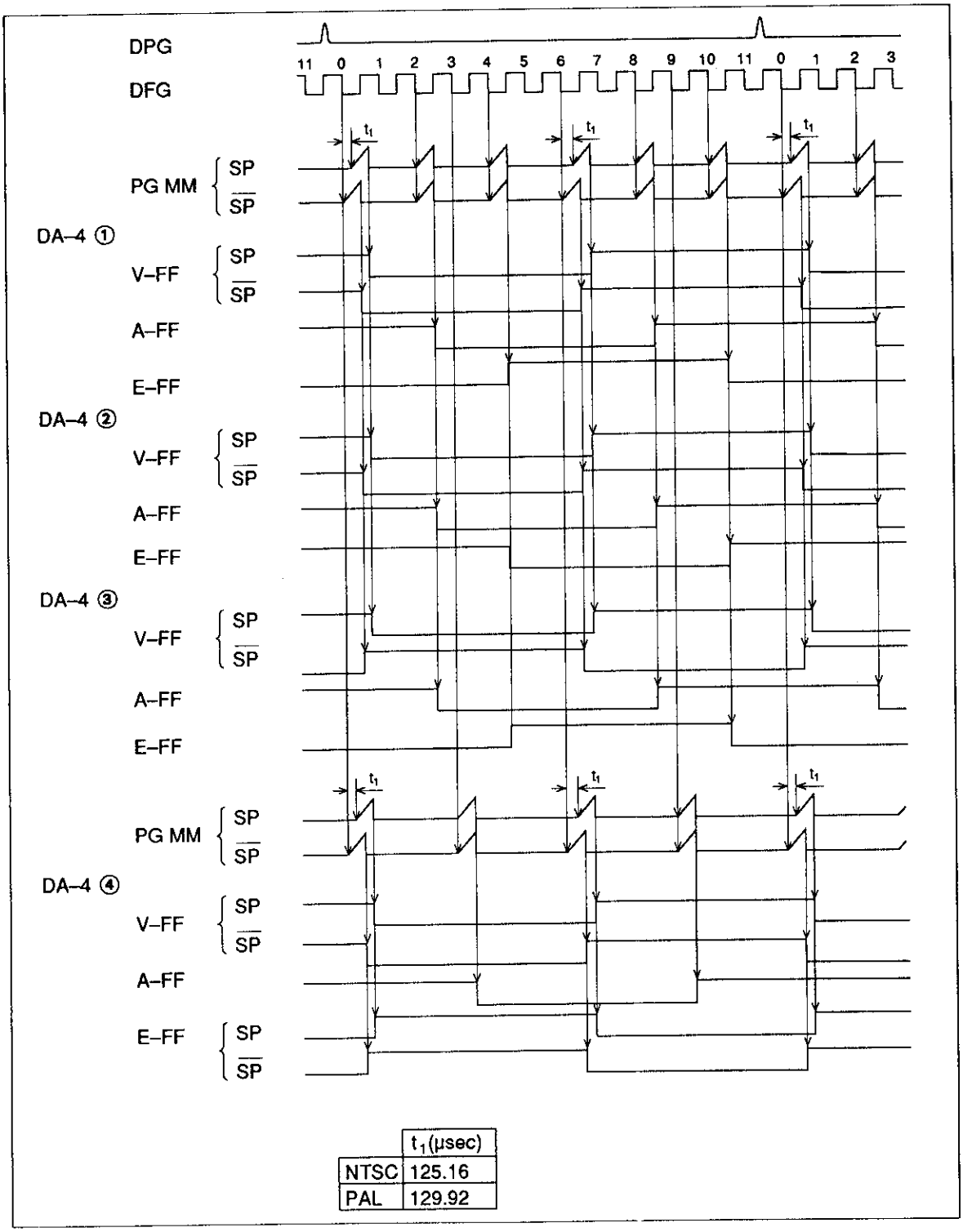
Control Timing Chart

Values in parentheses are for HD49733NT. N = NTSC/P = PAL

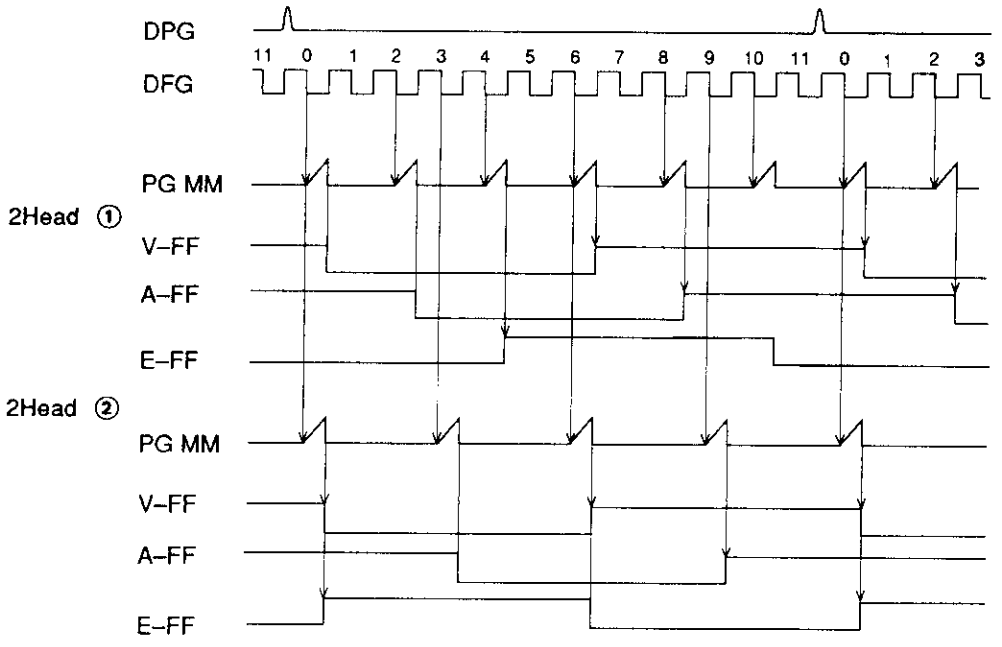


Head Switching System Control Timing Chart (HD49741NT)

$\overline{SP}$ = LP or EP mode
Head switching signal



	t_1(μsec)
NTSC	125.16
PAL	129.92



HD49741NT

A ⑩ / B ⑪	H	M	L
H	2Head ①	2Head ②	DA-4④
M	DA-4①	DA-4②	DA-4③
L	DA-4① TEST	DA-4② TEST	DA-4③ TEST

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	HD49733NT	HD49741NT	Unit
Supply voltage	V_{DD}	7.0	7.0	V
Operating supply voltage	V_{opr}	4.5 to 6.0	4.5 to 6.0	V
Storage temperature	T_{stg}	–40 to 125	–40 to 125	°C
Operating temperature	T_{opr}	–10 to 70	–10 to 70	°C
Power dissipation	P_T	500	500	mW

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C)

No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
1	Supply current	I_{CC}	8.0	20.0	32.0	mA	Quiescent Pins 28 and 38 total	28, 38		
2	2-value output voltage	V_{OL}	—	0.0	0.05	V	Quiescent	1 to 4, 44 to 47 49, 55, 56		
3	Same as above	V_{OH}	4.9	5.0	—	V	Quiescent	Same as above		
4	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 2mA	Same as above		
5	Same as above	V_{IH}	3.8	4.4	—	V	Load current = 2mA	Same as above		
6	Pull up output voltage	V_{OL}	0.0	0.1	0.3	V	No load	39, 40		
7	Same as above	V_{OH}	4.9	5.0	—	V	No load	39, 40		
8	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 2mA	39, 40		
9	Pull up resistance	R_H	6.0	9.0	13.0	kΩ		39, 40		
10	3-value output voltage	V_{OL}	0.0	0.2	0.4	V	No load	48		
11	Same as above	V_{OM}	2.3	2.5	2.8	V	No load	48		
12	Same as above	V_{OL}	4.6	4.8	5.0	V	No load	48		
13	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 1mA	48		
14	Same as above	V_{IH}	3.8	4.4	—	V	Load current = 1mA	48		
15	3-value output M level output impedance	R_M	6.0	9.0	13.0	kΩ		48		
16	REC CTL output pin-to-pin voltage	V_{CTL}	4.4	4.6	4.8	V	No load Voltage between pins 29 and 30	29, 30		
17	REC CTL output impedance	R_{CTL}	300	500	1000	Ω	I < 3mA Pins 29 and 30 total	29, 30		
18	2-value input V_{TH}	V_{TH}	1.5	2.5	3.5	V		19, 40, 41, 53, 54 (40, 41, 52, 53, 54)		
19	2-value input pull up resistance 1	R_{H1}	6.0	9.0	13.0	kΩ		40, 41, 53, 54		
20	2-value input pull up resistance 2	R_{H2}	24.0	36.0	52.0	kΩ		19 (52)		

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C) (cont)

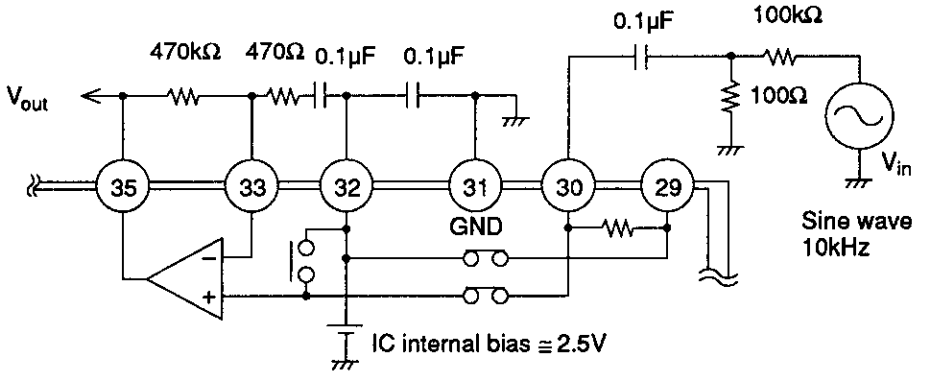
No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
21	3-value input V_{TH}	V_{TH1}	1.0	1.4	1.9	V	L/M V_{TH}	(9 to 11, 19, 15) 10, 11, 51		
22	3-value input V_{TH}	V_{TH2}	3.1	3.5	4.0	V	M/H V_{TH}	Same as above		
23	3-value input pin voltage	V_M	2.0	2.5	2.9	V		Same as above		
24	3-value input resistance	R_{M1}	18.5	28.0	42.0	kΩ		Same as above (10, 11, 19, 51)		
25	3-f_{sc} input sensitivity	V_{3fsc}	—	—	350	mV_{pp}		42		
26	f_{sc} input sensitivity	V_{fsc}	—	—	150	mV_{pp}		42		
27	Schmitt input pin voltage 1	V_{IS1}	2.2	2.5	2.8	V		36		
28	CTLP Schmitt input V_{TH}	V_{+TH1}	100	130	160	mV_p	Normal speed	36		
29	Same as above	V_{-TH1}	–160	–130	–100	mV_p	Normal speed	36		
30	Same as above	V_{+TH2}	200	260	320	mV_p	Mid-speed search	36		
31	Same as above	V_{-TH2}	–320	–260	–200	mV_p	Mid-speed search	36		
32	Same as above	V_{+TH3}	420	500	580	mV_p	High-speed search	36		
33	Same as above	V_{-TH3}	–580	–500	–420	mV_p	High-speed search	36		
34	Schmitt input pin voltage 2	V_{IS2}	2.3	2.7	3.1	V		9, 37		
35	FG Schmitt input V_{TH}	V_{+TH}	100	250	400	mV_p		9, 37		
36	Same as above	V_{-TH}	–30	0	30	mV_p		9, 37		
37	Schmitt input pin voltage 3	V_{IS3}	1.8	2.2	2.6	V		7		
38	PG Schmitt input V_{TH}	V_{+TH}	0.5	0.8	1.1	V		7		
39	Same as above	V_{-TH}	0.2	0.4	0.6	V		7		
40	Analog SW ON-state resistance	R_{ASW}	150	300	500	Ω		15 to 18, 22 to 26 29, 30, 32, 34, 35		

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C) (cont)

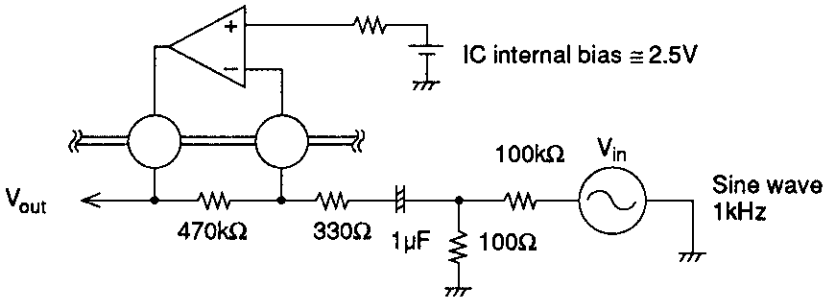
No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
41	Power on reset input V_{TH}	V_{52TH}	2.9	3.5	4.1	V		52		
42	Power on reset pull up resistance	R_{52}	24.0	36.0	52.0	kΩ		52		
43	Sync input V_{TH}	V_{50TH}	1.5	2.5	3.5	V	DC input	50		
44	Sync input pin voltage	V_{50}	1.8	2.4	3.0	V		50		
45	Sync input sensitivity	V_{SYC}	90	140	190	mV_p	Peak value from pin voltage for capacitive coupling.	50		
46	Sync input impedance	R_{50}	18.5	28.0	42.0	kΩ		50		
47	Mono-multi V_{TH}		—	2.5	—	V	Each mono/multi V_{TH}	5,6		
48	CTLP Amp Gain	A_{CTL}	57	60	62	dB	f = 10kHz		1	
49	CTLP Amp Gain	A_{CILO}	—	85	—	dB	Open loop gain			
50	DRUM ADD Amp Gain	A_D	57	60	62	dB	f = 1kHz		2	
51	Same as above	A_{D0}	—	85	—	dB	Open loop gain			
52	CAPSTAN ADD Amp Gain	A_C	57	60	62	dB	f = 1kHz		2	
53	Same as above	A_{C0}	—	85	—	dB	Open loop gain			

Test Circuit

1



2



$$\text{Gain} = 20 \log \frac{V_{out}}{V_{in}} + 60\text{dB}$$

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C) (HD49733)

No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
1	Supply current	I_{CC}	8.0	20.0	32.0	mA	No load Pins 28 and 38 total	28, 38		
2	2-value output voltage	V_{OL}	—	0.0	0.05	V	No load	1 to 4, 44 to 47 49, 55, 56		
3	Same as above	V_{OH}	4.9	5.0	—	V	No load	Same as above		
4	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 2mA	Same as above		
5	Same as above	V_{IH}	3.8	4.4	—	V	Load current = 2mA	Same as above		
6	Pull up output voltage	V_{OL}	0.0	0.1	0.3	V	No load	39, 40		
7	Same as above	V_{OH}	4.9	5.0	—	V	No load	39, 40		
8	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 2mA	39, 40		
9	Pull up resistance	R_H	6.0	9.0	13.0	kΩ		39, 40		
10	3-value output voltage	V_{OL}	0.0	0.2	0.4	V	No load	48		
11	Same as above	V_{OM}	2.3	2.5	2.8	V	No load	48		
12	Same as above	V_{OH}	4.6	4.8	5.0	V	No load	48		
13	Same as above	V_{IL}	—	0.6	1.2	V	Load current = 1mA	48		
14	Same as above	V_{IH}	3.8	4.4	—	V	Load current = 1mA	48		
15	3-value output M level output impedance	R_M	6.0	9.0	13.0	kΩ		48		
16	REC CTL output pin-to-pin voltage	V_{CTL}	4.4	4.6	4.8	V	No load Voltage between pins 29 and 30	29, 30		
17	REC CTL output impedance	R_{CTL}	300	550	1000	Ω	I < 3mA Pins 29 and 30 total	29, 30		
18	2-value input V_{TH}	V_{TH}	1.5	2.5	3.5	V		40, 41, 52, 53, 54		
19	2-value input pull up resistance 1	R_{H1}	6.0	9.0	13.0	kΩ		40, 41, 53, 54		
20	2-value input pull up resistance 2	R_{H2}	24.0	36.0	52.0	kΩ		52		

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C) (HD49733)

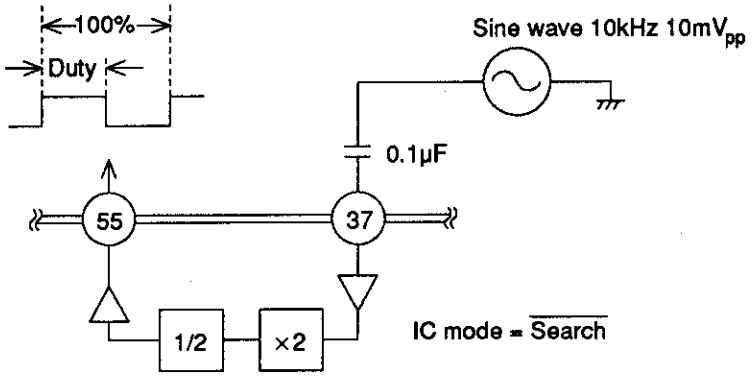
No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
21	3-value input V_{TH}	V_{TH1}	1.0	1.4	1.9	V	L/M V_{TH}	9 to 11, 19, 51		
22	3-value input V_{TH}	V_{TH2}	3.1	3.5	4.0	V	M/H V_{TH}	9 to 11, 19, 51		
23	3-value input pin voltage	V_M	2.0	2.5	2.9	V		9 to 11, 19, 51		
24	3-value input resistance 1	R_{M1}	18.5	28.0	42.0	kΩ		10, 11, 19, 51		
25	3-value input resistance 2	R_{M2}	6.5	9.4	13.5	kΩ		9		
26	3-f_{sc} input sensitivity	V_{3fsc}	—	—	350	mV_{pp}		42		
27	f_{sc} input sensitivity	V_{fsc}	—	—	150	mV_{pp}		42		
28	Schmitt input pin voltage	V_{IS}	2.2	2.5	2.8	V		36, 37		
29	CTLP Schmitt input V_{TH}	V_{+TH1}	100	130	160	mV_p	Normal speed	36		
30	Same as above	V_{-TH1}	100	130	160	mV_p	Normal speed	36		
31	Same as above	V_{+TH2}	200	260	320	mV_p	Mid-speed search	36		
32	Same as above	V_{-TH2}	200	260	320	mV_p	Mid-speed search	36		
33	Same as above	V_{+TH3}	420	500	580	mV_p	High-speed search	36		
34	Same as above	V_{-TH3}	420	500	580	mV_p	High-speed search	36		
35	CFG Schmitt input duty ratio	DR	45	50	55	%		37	1	
36	Analog SW ON-state resistance	R_{ASW}	150	300	500	Ω		15 to 18, 22 to 26 29, 30, 32, 34, 35		
37	CTLP Amp Gain	A_{CTL}	57.0	60.0	62.0	dB	f = 10kHz		2	
38	CTLP Amp Gain	A_{CTLO}	—	85	—	dB	Open loop gain			
39	DRUM ADD Amp Gain	A_D	57.0	60.0	62.0	dB	f = 1kHz		3	
40	Same as above	A_{DO}	—	85	—	dB	Open loop gain			

Electrical Characteristics (V_{CC} = 5V, Ta = 25°C) (HD49733)

No.	Test Item	Symbol	Min	Typ	Max	Unit	Test Condition	Applicable Pin	Test Circuit	Note
41	CAPSTAN ADD Amp Gain	A_C	57.0	60.0	62.0	dB	f = 1kHz		3	
42	Same as above	A_{CO}	—	85	—	dB	Open loop gain			
43	Pin 50 DC input V_{TH}	V_{TH50}	1.8	2.5	3.0	V		50		
44	Pin 50 bias potential	V_{50}	0.5	1.0	1.5	V		50		
45	Pin 50 capacitive coupling input sensitivity	V_{SYNC}	—	1.5	2.5	V_p		50		
46	Pin 50 input resistance	R_{50}	20	43	80	kΩ		50		
47	Mono-multi V_{TH}		—	2.5	—	V	Each mono-multi V_{TH}			
48	Pin 6 applied voltage	V_6	—	—	3.1	V	Approved applied voltage			

Test Circuit

1



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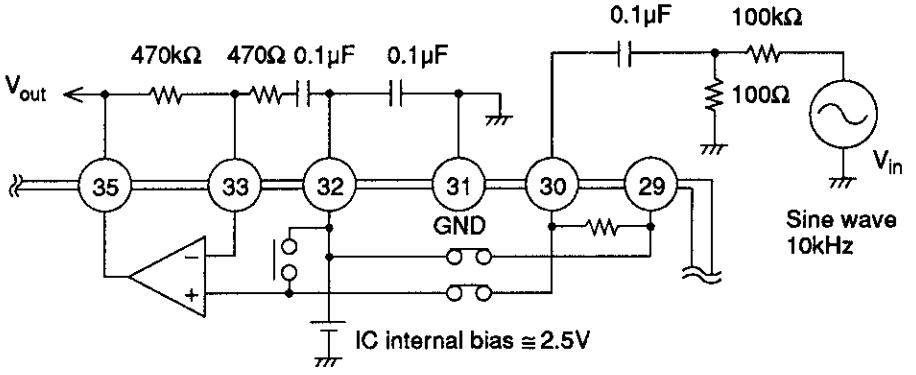
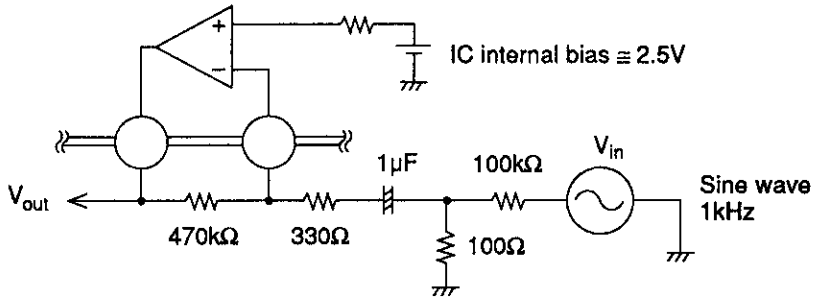


$$\text{Gain} = 20 \log \frac{V_{out}}{V_{in}} + 60\text{dB}$$

3



Appendix A — Comparison of HD49741 and HD49733

General

HD49741 and HD49733 are Hitachi CMOS servo LSI base chips. Though their functions are basically the same, these two chips have some differences. Note that even for functions that are the same for both chips, their pin numbering differs, as do their mode pins and functions.

The following are the main differences between the two chips:

- HD49741 has two individual pins for PG and DFG input, while HD49733 has one pin
- HD49733 has a on-chip doubler for CFG input, and CFG frequency can be set in the range of 360 to 1440Hz

Both HD49741 and HD49733 are available in the DP-56S package.

The following chart shows the functional differences between HD49741 and HD49733. Chip selection should be made based on the motor requirements of the system.

	Item	HD49741	HD49733	See paragraph
1	PG, DFG input	One pin each (2 pins total)	One pin, combined input	1
2	CFG input	Detection at fall only	Detection at rise and fall (on-chip doubler)	2
3	Extra-FF output	Yes	No	
4	Ex-reset	Special pin (Pin 51)	Input along with C-sync input (Pin 50)	3
5	TR TRG (tracking trigger output)	Yes	No	—
6	Supplemental V output	2 pins (Pins 48, 49)	1 pin (Pin 48)	4
7	YNR output	No	Yes	5
8	Frame shift	No	Yes	6
9	Mode output	ABCDE	A, B, C, D, E(CFG C/D out CTLP C/D out)	7
10	Supplemental V delay shift	Serial control	Externally added 6H fixed CR mono-multi and combinations	8

PG, DFG input

With HD49741, Pin 7 is used for PG input, while Pin 9 is used for DFG input. With HD49733, on the other hand, a composite signal is input at Pin 9. The following illustrates the necessary input waveform.

Note also that Pin 9 has a bias of approximately 2.5V at 10kΩ typ. V_{TH} is 1.1 to 2.0V for DFG, and 2.9 to 3.8V for PG (when V_{CC} = 5V).

CFG input

HD49741 performs speed control (also used internally by the IC during recording as CFG 30 for phase control) based on the CFG's falling edge only. With HD49733, on the other hand, control is based on both the rising edge and falling edge (doubler). This means that HD49733 is best when CFG duty of 50% and higher precision are desirable. Since HD49733 has a built-in doubler, the CFG frequency can be set within the range of 360Hz to 1440Hz (in accordance with the optional setting of mask ROM).

Ex-reset

HD49741 is equipped with an EX-RESET pin (Pin 51) for external synchronization of the servo IC Ref-30 for VTRs with frame memory. In order to reduce the total number of pins, input on HD49733 is performed at the same pin used for C-sync input (Pin 50), since C-sync is not used in memory applications. Serial control is used to specify whether Pin 50 is to be used as a C-SYNC pin or EX-RESET pin. Switching of the connection with luminance IC and memory controller should be performed using an external analog switch.

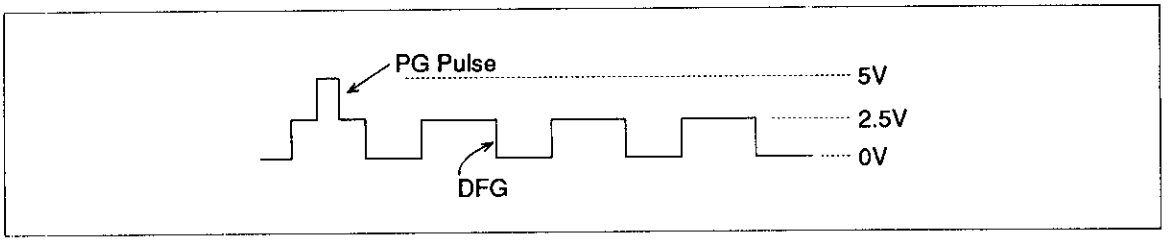
Supplementary V output

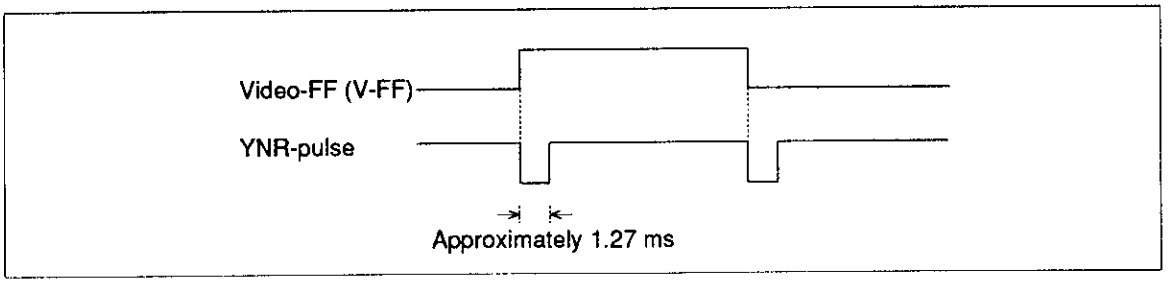
Pin 48 (VP) and Pin 49 (HD) of HD49741 are used for supplementary V output. Pin 48 and 49 output can be adjusted by external resistance in accordance with the threshold of the luminance IC that inputs the V pulse. When only Pin 48 is used, however, this pin outputs the three values of 0, 2.5V and 5.0V.
With HD49733, a 3-value output is performed at Pin 48.

YNR output

HD49733 is equipped with YNR output (Pin 47) to switch OFF the YNR of the luminance signal processor. YNR is output within the period approximately 1.27ms from the video-FF rise and fall points, in all modes except the supplementary VON mode.

Pin 47 is LOW in modes that do not use the YNR-pulse.





Frame shift

HD49733 is equipped with an output pin called a frame shift (Pin 19). This pin should normally be kept OPEN. When this pin is externally forced to the LOW level, capstan phase control does not operate (fixed at VPD/2), and capstan speed control only is operational.
When H level is supplied to this pin, capstan phase control does not operate and capstan speed control only operates, but capstan speed control is set to a level some percent slower than normal control.

Mode output

HD49741 mode output includes A, B, C, D, E and Pin 5 output. A to E signal output is selectable using serial control (see Serial Control).
With HD49733, mode output signals are A, B, C, D, whose contents are determined by serial control input, and fixed CFG C/D output as well as fixed CTLP C/D output used to discriminate the SP/LP/EP mode. Note that the meaning of the A, B, C, D, output signal for HD49733 differs from that of HD49741. For details, see On-chip Functions.

Supplementary V delay shift

Supplementary V delay shift for HD49741 is performed using serial control to specify a value. For details, see On-chip Functions.
With HD49733, delay amount can be selected from a fixed delay amont (6H) or a mono-multi vibrator delay amount, determined with the additional CR to Pin 6 for CH1 and CH2 respectively. Serial control is used to select CH1 or CH2.

Differences in Drum Select A and Drum Select B Encoding

Though both chips allow selection from among 9 types of head configuration, the head format selections differ. For details, see Pin Functions.

Comparison of HD49741 and HD49733 Pin Arrangements

Pin No.	HD49741	HD49733
1	Tracking trigger output	Mode D output
6	RC pin for PG MM	RC pin for VP MM
7	DPG input	RC pin for PG MM
9	DFG input	DPG/FG input
19	NTSC/PAL switch input	Frame shift specification input
45	Video-FF output	Audio-FF output
46	Audio-FF output	Video-FF output
47	Extra-FF output	YNR-pulse output
49	HD output	Mode # output
50	COMP-SYNC input	COMP-SYNC/Ext. Ref input
51	Ext. reset input	NTSC/PAL/SECAM switch input
55	Mode D output	CFG C/D output
56	Mode E output	CTL C/D output

Current Lineup

Besides HD49741/HD49733, the VCR servo ICs listed below are also available for various CFG and DFG frequencies.

Model	CFG Frequency (NTSC/SP modes)	DFG Frequency
HD49747	2160 Hz	360 Hz
HD49748	1080 Hz	720 Hz
HD49750	1080 Hz	720 Hz
HD49756	2160 Hz	720 Hz
HD49754	720 Hz	720 Hz