

Prepared		Product Specifications AN17850A	Ref No.	A
Checked			Total Page	17
Approved			Page No.	1

Structure	Silicon Monolithic Bipolar IC
Appearance	SIL-12 Pins Plastic Package (FP-12S Power Type With Fin)
Application	Audio
Function	70W (6Ω) x 1ch BTL Power Amplifier Built-in Standby and Muting Features Incorporating Various Protection Circuits

A	Absolute Maximum Ratings				
No.	Item	Symbol	Ratings	Unit	Note
1	Storage Temperature	Tstg	-55 ~ +150	° C	
2	Operating Ambient Temperature	Topr	-25 ~ +75	° C	
3	Operating Ambient Pressure	Popr	1.013x10 ⁵ ±0.61x10 ⁵	Pa	
4	Operating Constant Acceleration	Gopr	9,810	m / s ²	
5	Operating Shock	Sopr	4,900	m / s ²	
6	Power Supply Voltage	Vcc	33	V	1
7	Power Supply Current	Icc	8.0	A	
8	Power Dissipation	PD	37.5	W	2

Operating Supply Voltage Range	Vcc	10 V ~ 32V
--------------------------------	-----	------------

Note: 1) Without input signal, Vcc is up to 33V
2) Ta = 75°C with infinite heatsink

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications AN17850A	Ref No.	B-1
Checked			Total Page	17
Approved			Page No.	2

No.	Item	Symbol	Test Circuit.	Condition	Limit			Unit	Note
					Min	Typ	Max		
1	Quiescent Circuit Current	I _{cq}	1	No input ; V _{stby} = 5V V _{mute} = 5V;	-	100	300	mA	
2	Output Noise Voltage	V _{no}	1	No Input, R _g =20kΩ V _{stby} = 5V;V _{mute} = 5V	-	0.54	1	mV _{rms}	1
3	Voltage Gain	G _{vc}	1	V _{in} =20mV; V _{stdby} =5V V _{mute} = 5V	38	40	42	dB	
4	Total Harmonic Distortion	THD	1	V _{in} =20mV; V _{stdby} =5V V _{mute} = 5V;	-	0.07	0.4	%	2
5	Maximum Output Power	P _o	1	THD _{OUT} =10% V _{stdby} =5V;V _{mute} = 5V;	55	70	-	W	
6	Output Offset Voltage	V _{off}	1	R _g =20kΩ; No input V _{stdby} =5V;V _{mute} =5V;	-350	0	350	mV	
7	Ripple Rejection	RR	1	V _{ripple} =1V _{rms} * freq=120Hz, R _g =20kΩ	45	55	-	dB	1
8	Standby Current	I _{STB}	1	No input ; v _{stdby} =0V; V _{mute} =5V;	-	1	100	μA	
9	Muting Effects	MT	1	V _{in} =20mV; V _{stby} =5V; V _{mute} = 0 to 5V**	65	75	-	dB	2

* The measurement is by taking the ratio of output voltage with reference to the V_{ripple}.

** The measurement is by taking the ratio of output (at V_{mute} = 0 V) to the output(at V_{mute} = 5V)

Note : 1) With a filter band 20Hz ~20kHz (12 dB/OCT) used.

2) With a filter band 400Hz ~30kHz used.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications (Reference Data for Design) AN17850A	Ref No.	B-2
Checked			Total Page	17
Approved			Page No.	3

B Electrical Characteristics		(Unless otherwise specified, the ambient temperature is 25°C±2°C, Vcc=30V, frequency=1kHz and RL=6Ω.)							
No	Item	Symbol	Test Circuit	Conditions	Limits			Unit	Note
					min	typ	max		
1	Standby on voltage	Vstdon	1	Vmute = 5V; Vin = 20mV; Istb < 100uA	-	-	1	V	
2	Standby off voltage	Vstdoff	1	Vmute = 5V; Vin = 20mV; Gvc > 38 dB	4.5	-	-	V	
3	Mute on voltage	Vmon	1	VStdby = 5V; Vin = 20mV; MT > 70 dB	-	-	1	V	
4	Mute off voltage	Vmoff	1	VStdby = 5V; Vin = 20mV; Gvc > 38 dB	4	-	-	V	

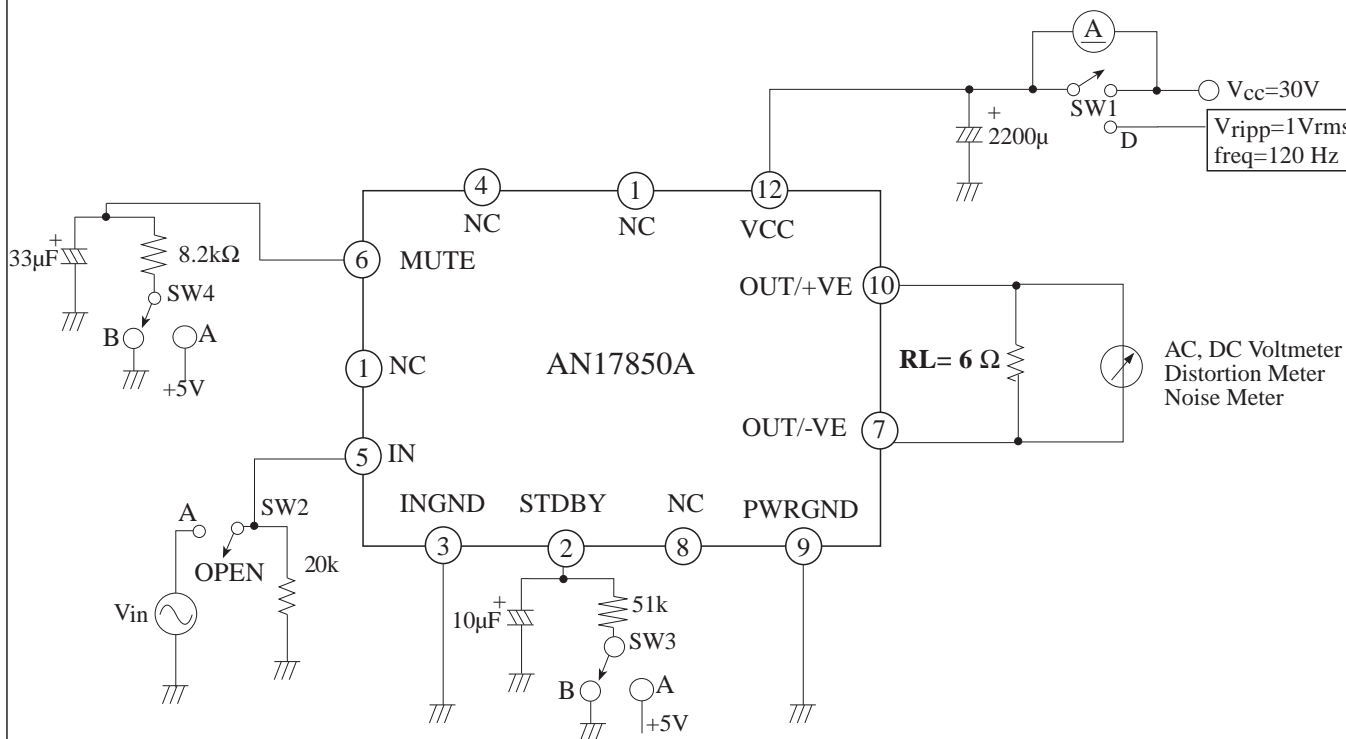
Note) The above characteristics are reference values determined for IC design, but not guaranteed values for shipping inspection. If problems were to occur, counter measures will be sincerely discussed.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications AN17850A	Ref No.	C
Checked			Total Page	17
Approved			Page No.	4

(Description of Test Circuits and Test Methods)

Test Circuit 1



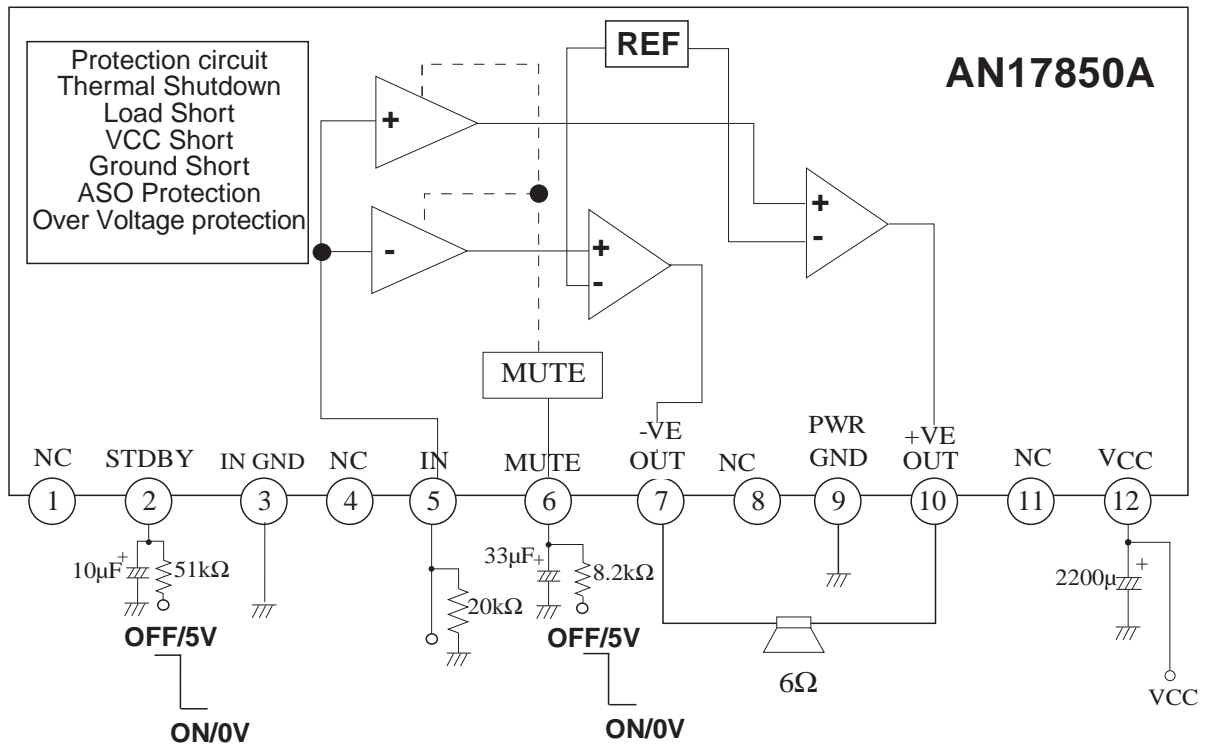
No.	Item	SW1	SW2	SW3	SW4
1	I _{cq}	OPEN	OPEN	A	A
2	V _{no}	Closed	OPEN	A	A
3	G _{vc}	Closed	A	A	A
4	THD	Closed	A	A	A
5	PO	Closed	A	A	A
6	V _{off}	Closed	OPEN	A	A
7	R.R	D	OPEN	A	A
8	ISTB	OPEN	OPEN	B	A
9	MT	Closed	A	A	B/A

Note : * STB 'OFF' means 5V.
MUTE 'OFF' means 5V.

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications AN17850A	Ref No.	D
Checked			Total Page	17
Approved			Page No.	5

Circuit Function Block Diagram



Pin Descriptions

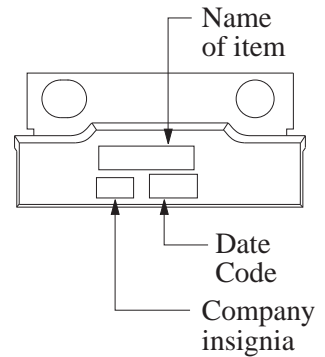
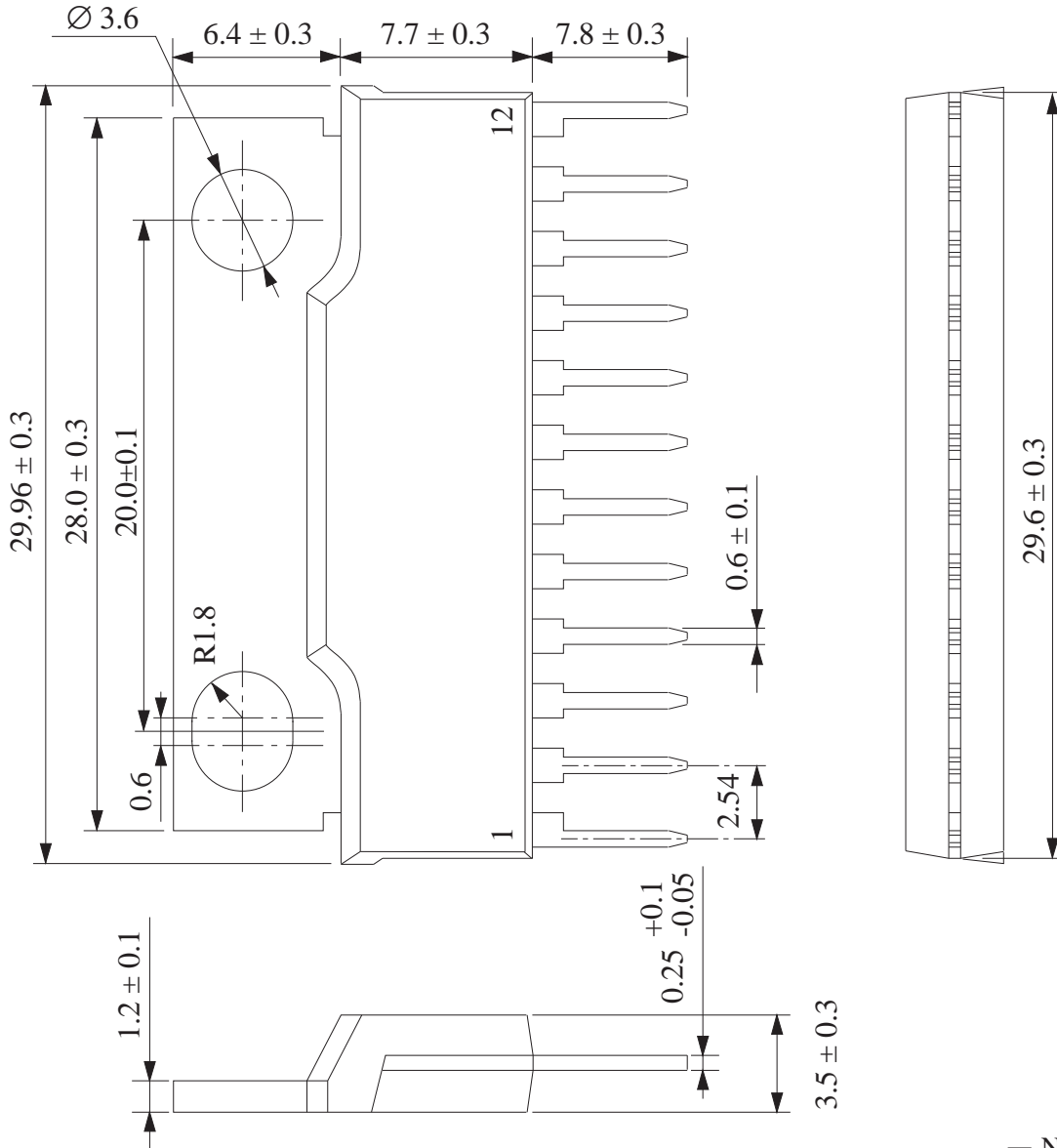
Pin No.	Pin Descriptions	Pin No.	Pin Descriptions
1	NC	7	-VE PHASE OUTPUT
2	STDBY	8	NC
3	IN GND	9	PWR GND
4	NC	10	+VE PHASE OUTPUT
5	IN	11	NC
6	MUTE	12	VCC

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications AN17850A	Ref No.	E
Checked			Total Page	17
Approved			Page No.	6

Package Name	FP-12S
--------------	--------

Unit : mm



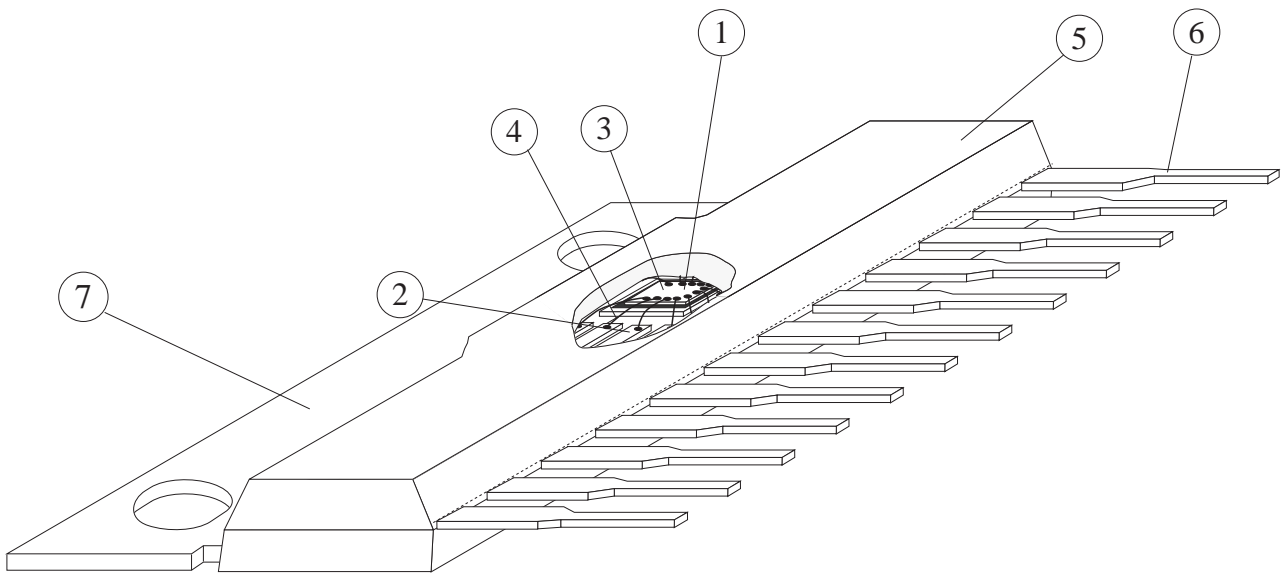
Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications AN17850A	Ref No.	F
Checked			Total Page	17
Approved			Page No.	7

(Structure Description)

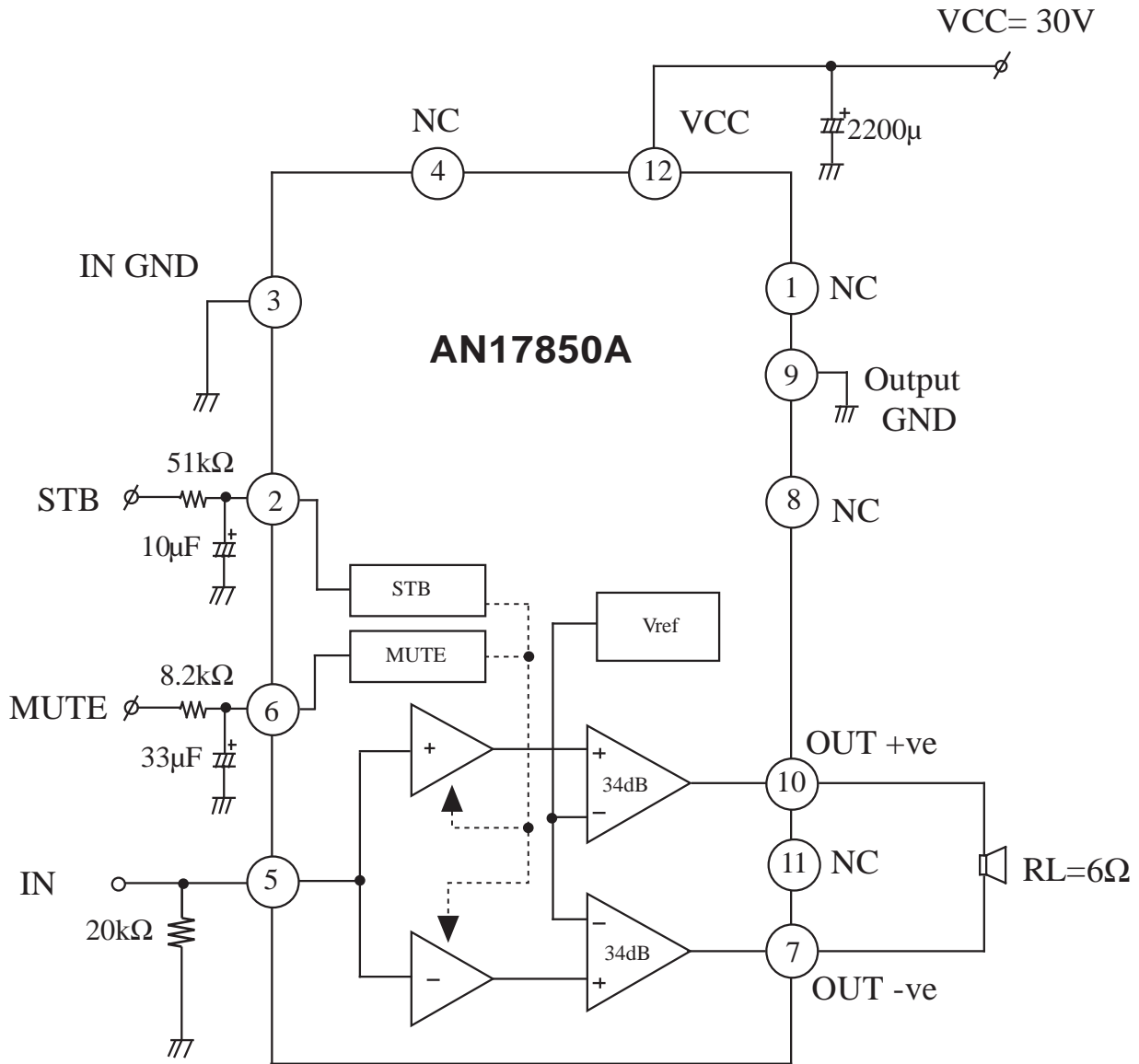
Chip surface passivation	SiN,	PSG,	Others ()	①	
Lead frame material	Fe group,	Cu group,	Others ()	②, ⑥	
Inner lead surface process	Ag plating,	Au plating,	Others ()	②	
Outer lead surface process	Solder plating,	Solder dip,	Others ()	⑥	
Chip mounting method	Ag paste,	Au-Si alloy,	Solder,	Others ()	③
Wire bonding method	Thermalsonic bonding,		Others ()	④	
Wire material	Au		Others ()	④	
Mold material	Epoxy,		Others ()	⑤	
Molding method	Transfer mold,	Multiplunger mold,	Others ()	⑤	
Fin material	Cu Group		Others ()	⑦	

Package FP-12S



Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Application Circuit



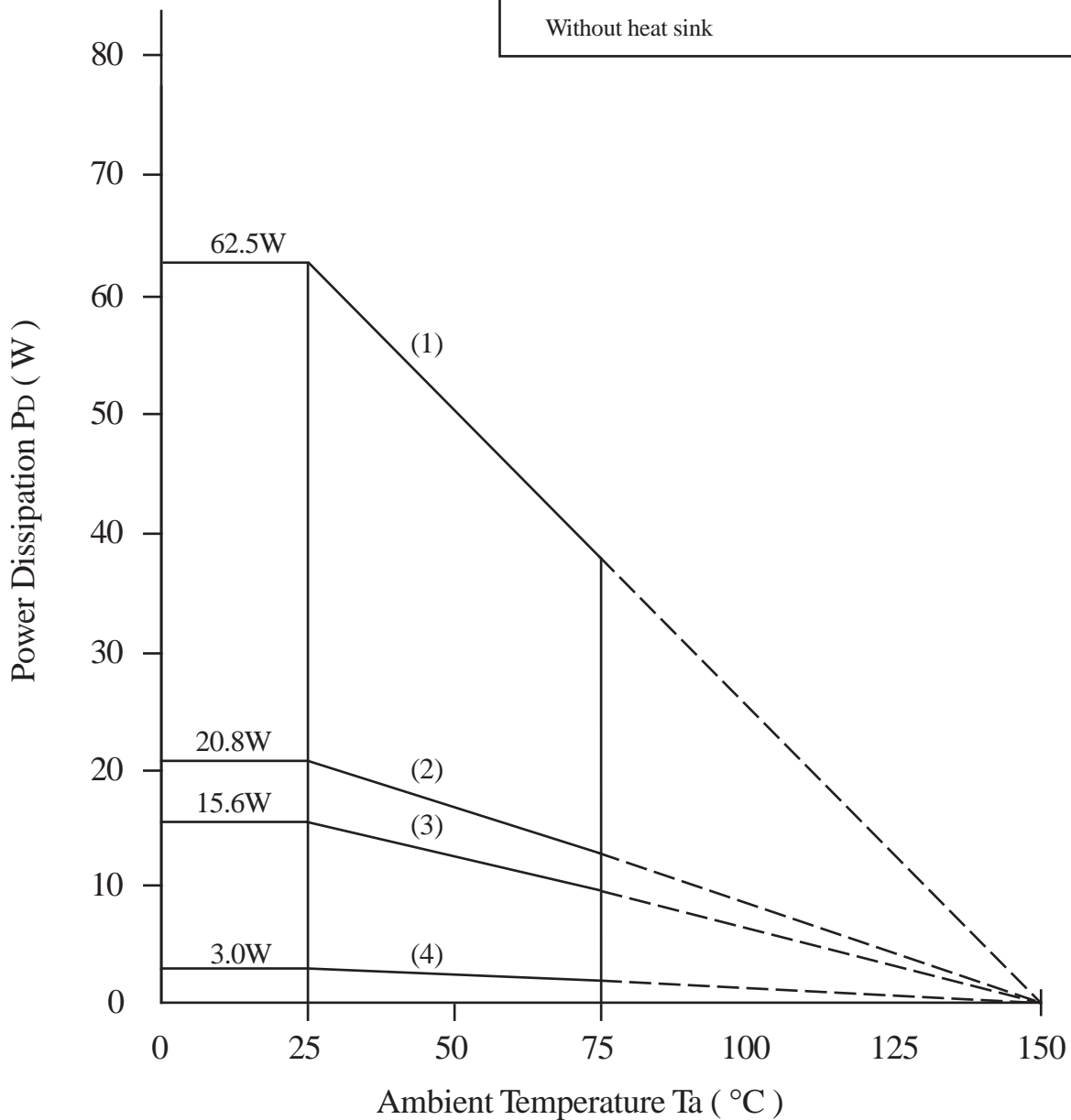
STB 'OFF'	5V
STB 'ON'	0V
Mute 'OFF'	5V
Mute 'ON'	0V

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-2
Checked			Total Page	17
Approved			Page No.	9

PD - Ta Curves

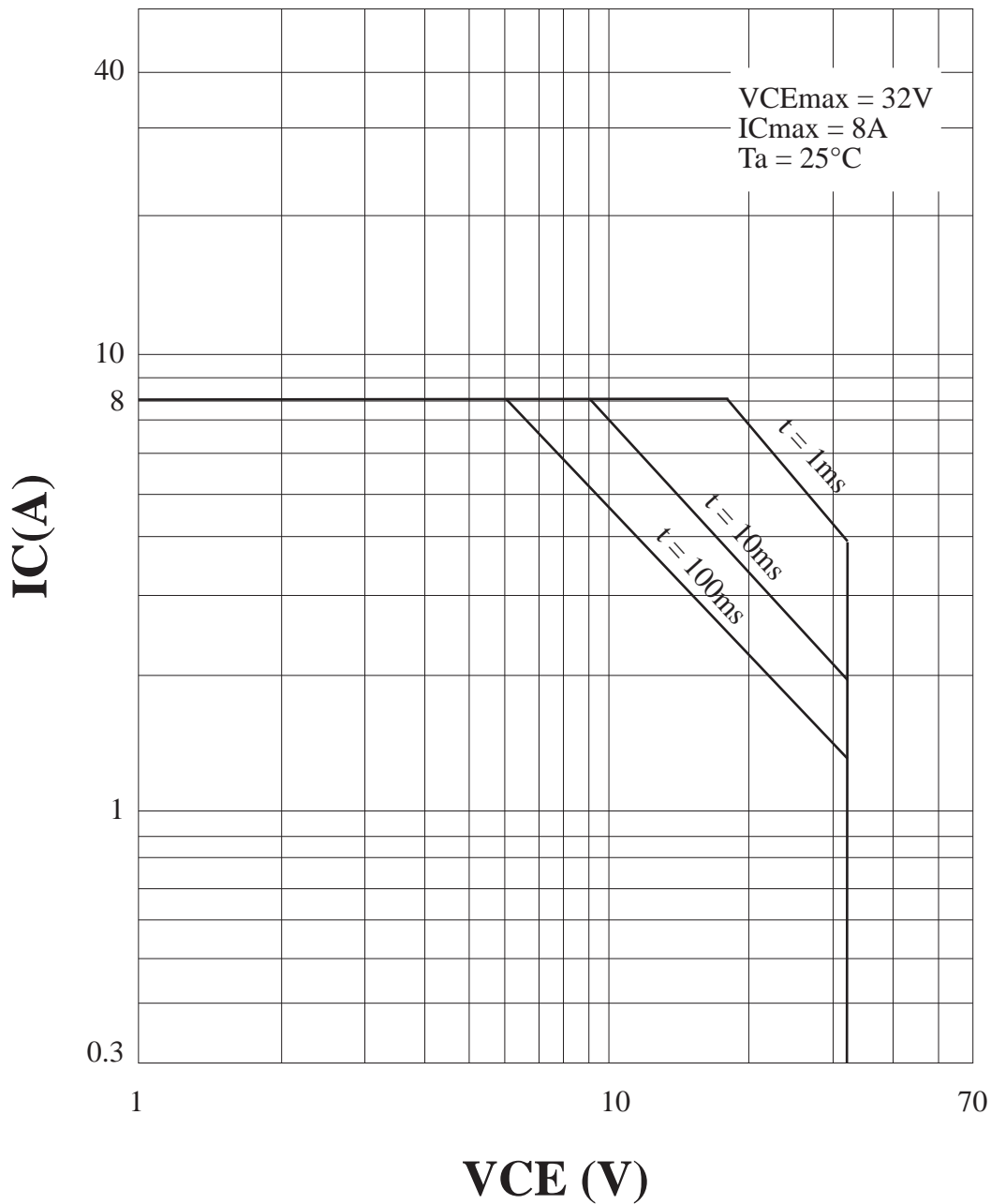
- (1) $T_c = T_a, 62.5W$ ($\theta_{j-c} = 2 \text{ }^\circ\text{C/W}$)
- (2) $20.83W$ ($\theta_f = 4.0 \text{ }^\circ\text{C/W}$)
 With a $100\text{cm}^2 \times 3\text{mm}$ Al heat sink (black colour coated)
 or a $200\text{cm}^2 \times 2\text{mm}$ Al heat sink (not lacquered)
- (3) $15.63W$ ($\theta_f = 6.0 \text{ }^\circ\text{C/W}$)
 With a $100\text{cm}^2 \times 2\text{mm}$ Al heat sink (not lacquered)
- (4) $3.0W$ at $T_a = 25^\circ\text{C}$ ($\theta_{j-a} = 42^\circ\text{C/W}$)
 Without heat sink



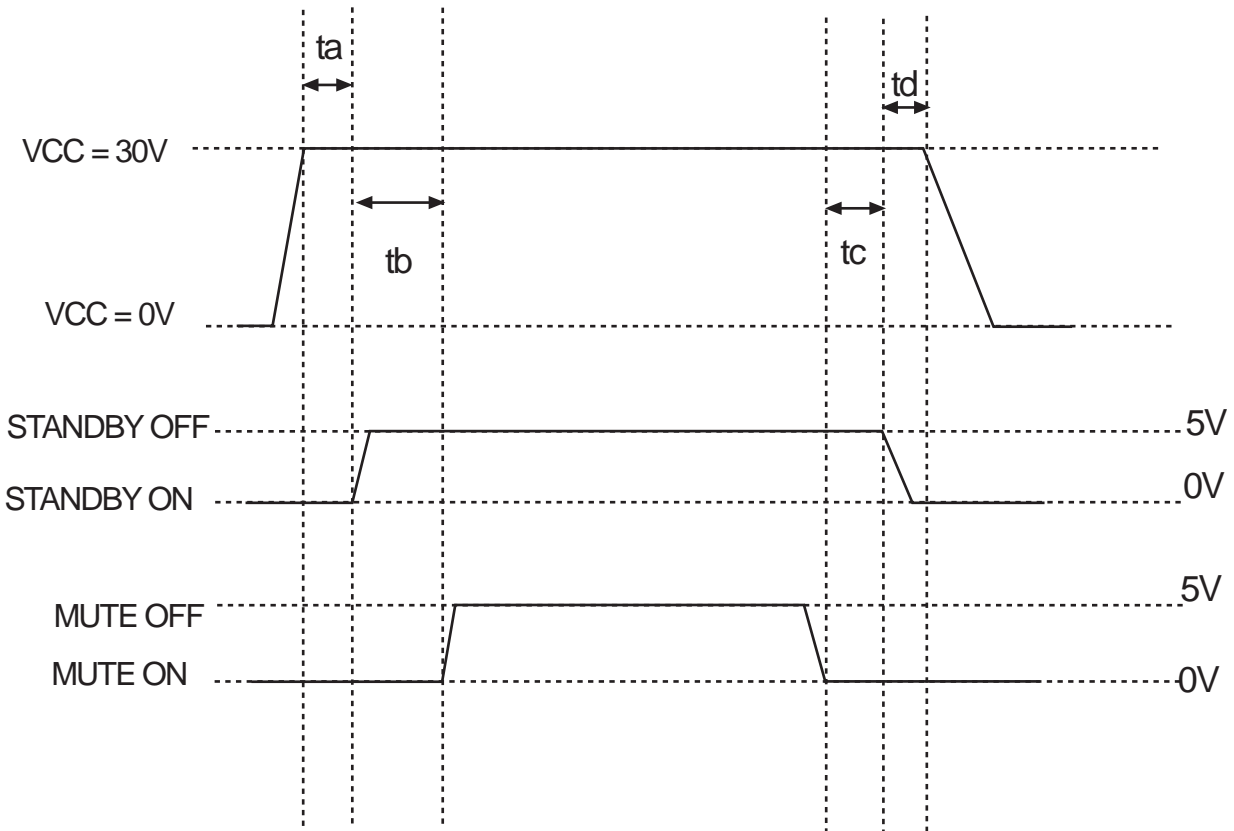
Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-3
Checked			Total Page	17
Approved			Page No.	10

Area of Safe Operation



Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				



	Description	Minimum	Unit
t_a	Waiting time required for Standby to turn off after VCC is on.	0	ms
t_b	Waiting time required for Mute turn off after Standby is off.	500	ms
t_c	Waiting time required for Standby to turn on after Mute is on	300	ms
t_d	Waiting time required for VCC to turn off after Standby is on	0	ms

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-5
Checked			Total Page	17
Approved			Page No.	12

Pin No.	Function	Internal circuitry	Description	DC BIAS (V)
1	NC	—	—	—
2	Standby		Standby control pin Standby "ON" = 0V Standby "OFF" = 5V	Determined by external
3	IN GND	—	Input ground	0V
4	NC	—	—	—
5	INPUT		AC input Terminal	0V
6	MUTE		MUTE Control MUTE "OFF" = 5V MUTE ON = 0V	Determined by external

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

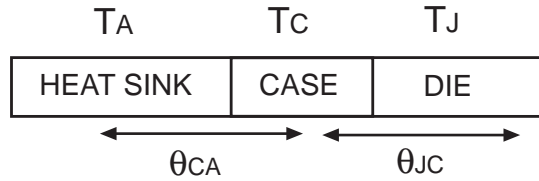
Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-5
Checked			Total Page	17
Approved			Page No.	13

Pin No.	Function	Internal circuitry	Description	DC BIAS (V)
7	Output (-)		Negative output terminal	VCC/2
8	NC	_____	_____	_____
9	PWR GND		Output Power Ground	0V
10	Output (+)		Positive output terminal	VCC/2
11	NC	_____	_____	_____
12	VCC		Power Supply Pin	Typ 30V

Eff. Date	Eff. Date	Eff. Date	Eff. Date
15-AUG-03			

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-6
Checked			Total Page	17
Approved			Page No.	14

Power dissipation and Heat Sink



Definition of terms

- PD: Power Dissipation
- Tj: Junction Temperature
- TC: Case Temperature
- TA: Ambient Temperature
- θJC: Thermal Resistance of junction to case
- θCA: Thermal Resistance of case to ambient, normally through heat sink

FIG1. Simplified Illustration of IC and Heat Sink attached

The following two equations represent the relations of these terms.

$$(T_j - T_c) / \theta_{JC} = P_D \quad (1)$$

$$(T_c - T_A) / \theta_{CA} = P_D' \quad (2)$$

For reliable and long-term, continuous operation, junction temperature should not exceed 125°C and θJC for FP-12S package is 2°C/W. Substitute these values in Equation 1. After specify the PD, Tc can be determined.

Assume no heat loss at the casing, i.e. all power is dissipated to the ambient through heat sink, which is quite true. So PD = PD'. Since Tc is also known, one can determine the following using equation2:

- a) The rating of heat sink for specific maximum operating ambient temperature, or
- b) The maximum operating ambient temperature for specific heat sink rating.

A more general equation can be used for rough calculation.

$$(T_J - T_A) / \theta_{JA} = P_D \quad (3)$$

$$\theta_{JA} = \theta_{CA} + \theta_{JC} \quad (4)$$

In this case, θJA is total thermal resistance of the heat sink and IC package. Therefore, for specified power dissipation, either heat sink rating or maximum operating ambient temperature can be decided if the other is known.

Take note that it's essential to know PD value before hand in order to work out other quantities. PD calculation is as shown.

$$P_D = V_{CC} \times I_{CC} - P_{o_total} \quad (5)$$

- Vcc: DC supply voltage
- Icc: RMS value of IC current
- Po_total: Total output power

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-6
Checked			Total Page	17
Approved			Page No.	15

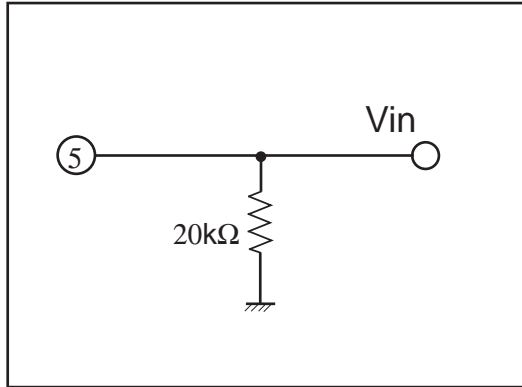


FIG2. Input DC Biasing

Input DC biasing

Input DC bias is maintained at ground level. If the input signal contains DC bias voltage, AC coupling should be included on the application circuit.

The value of 20kΩ resistor is set in order to achieve the minimum output DC offset.

Output Zobel Network

It should be noted that this device is designed such that the Zobel network (RC pair) at the output pins is not necessary for stable operation.

In practical application, the Zobel network may be applied optionally for two reasons:

- a) Ensuring stability for different PCB layout and speaker types.
- b) Ability to withstand to high ESD levels.

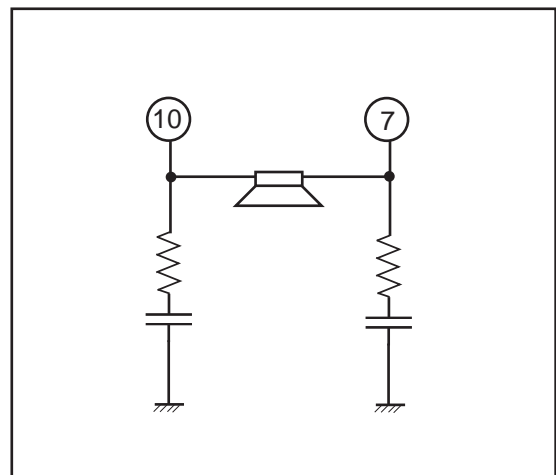


FIG3. Output Zobel Network

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications (Technical Data) AN17850A	Ref No.	G-6
Checked			Total Page	17
Approved			Page No.	16

Standby operation

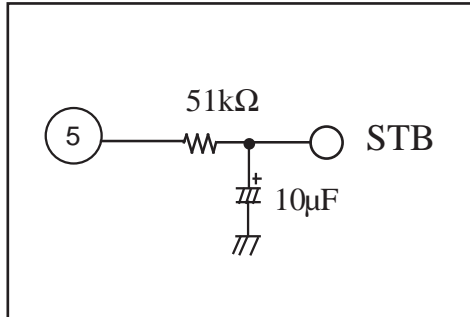


FIG4. Standby Application circuit

Standby pin should be connected with carefully selected components in order to avoid “Pop Noise” during Standby ON/OFF transient.

The 51k resistor and 10uF capacitor pair can delay the rising of voltage at pin 5 to reach the Standby threshold. When Standby is switching on together with supply, this delay would be very useful to ensure no “Pop Noise”.

If the Standby voltage is provided by a microcontroller, the suppression of “Pop” could even be better.

For further details of timing and delay for standby circuit, please refer to page 11.

Mute operation

Mute pin should be connected with carefully selected components in order to avoid “Pop Noise” during MUTE ON/OFF transient.

The 8.2k resistor and 33uF capacitor pair can delay the rising of voltage at pin 6 to reach the Mute threshold. When Mute is switching on together with supply, this delay would be very useful to ensure no “Pop Noise”.

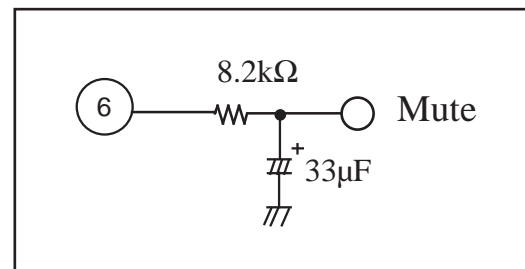


FIG5. Mute application circuit

For further details of timing and delay for Mute application circuit, please refer to page 11.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				

Prepared		Product Specifications AN17850A	Ref No.	H
Checked			Total Page	17
Approved			Page No.	17

(Precaution for use)

- 1) Ground the radiation fin so that there will be no difference in electric potential between the radiation fin and ground.
- 2) The thermal protection circuit operates at T_j at approximately 150°C. Thermal protection circuit is reset automatically when the temperature drops.
- 3) Be sure to attach heatsink to the IC before use. Make sure that the heatsink is secured to the chassis.
- 4) In order to prevent IC from being damaged during the fault test, prior to standby switching from on to off or vice versa, it is important to assert the mute on. Please refer to the timing diagram on page 11.

Eff. Date	Eff. Date	Eff. Date	Eff. Date	
15-AUG-03				